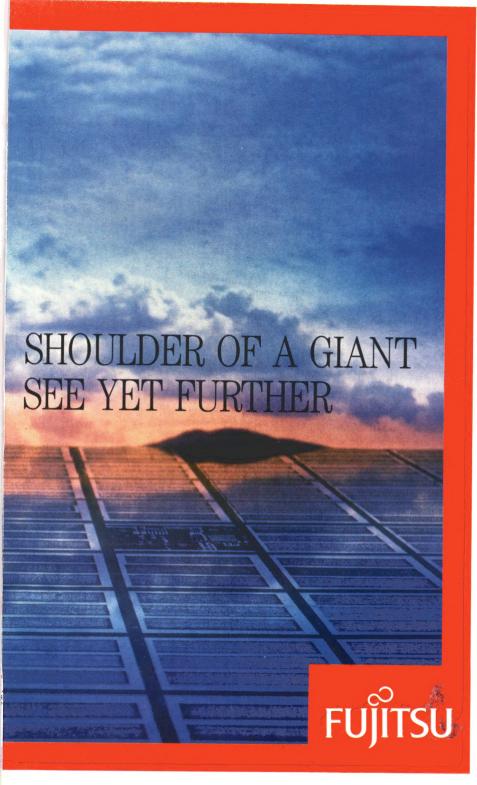
Troubleshooting analog circuits—Part 10

PC-board thermostats add design options

EISA vs Micro Channel

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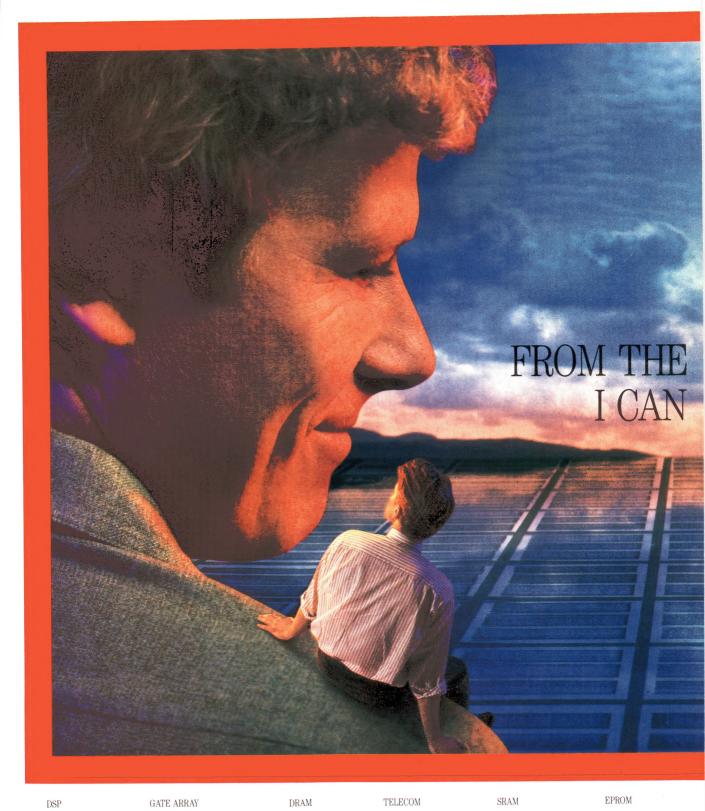








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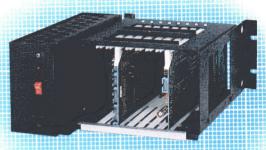
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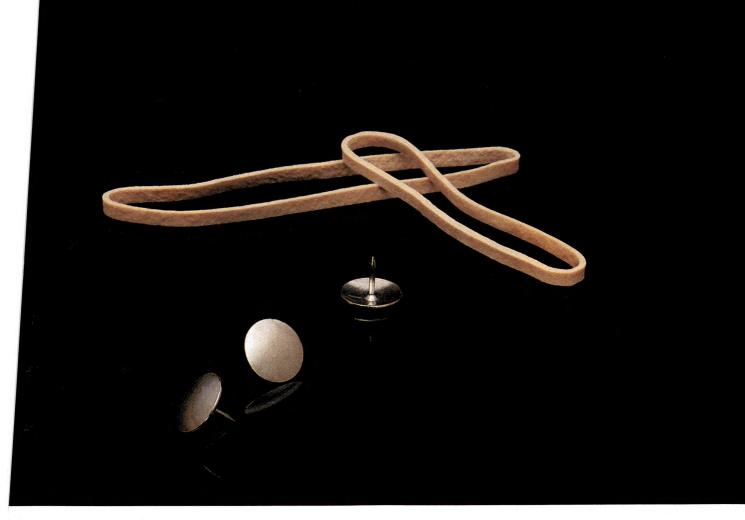
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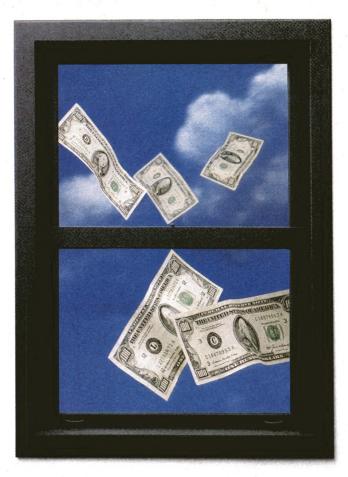
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Volume 34, Number 20



September 28, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: 8- and 16-bit microcontrollers are less expensive and more sophisticated than ever before, offering a wide variety of modular on chip peripherals that you can add to customize your device as your needs change. See the Special Report, beginning on pg 108. (Photo courtesy Motorola Inc; cover concept by Staats Falkenberg & Partners Inc; photography by Tomás Pantin)

SPECIAL REPORT

8- and 16-bit microcontrollers

108

Microcontroller prices are plunging. At the same time, manufacturers are increasing the variety of peripherals integrated on chip. The severe competition in the microcontroller market means that system designers can obtain a greater assortment of sophisticated, application-specific devices at cutthroat prices.

— J D Mosley, Regional Editor

DESIGN FEATURES

Designer's guide to microcontroller simulation 131 Part 1

Design-verification tests can tell you early on whether your product will perform as specified and whether your hardware and software will work smoothly together, even under worst-case conditions. This article shows how you can use a simulator to perform tests that would be difficult or impossible with standard hardware.—Anders Gezelius, Archimedes Software Inc

Troubleshooting analog circuits Part 10

145

The boundary between the analog and digital worlds confounds and frightens all too many engineers. Armed with the solid theoretical foundation and insights presented in this installment, you can keep your journey into the analog/digital world from seeming like a visit with Peter Pan.

— Robert A Pease, National Semiconductor Corp

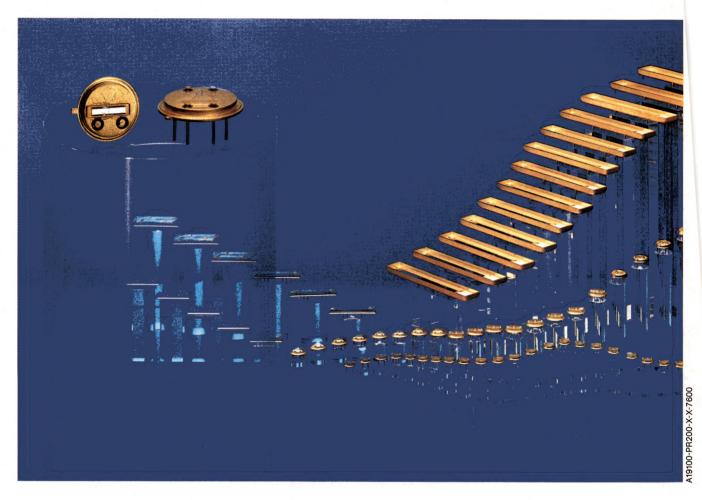
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As EISA enters the ring to challenge MCA, you should compare their capabilities before developing new boards for either bus (pg 75).

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TECHNOLOGY UPDATES

Thermostat packaging adds design flexibility

63

Today's high-density transistors and crowded surface-mount ICs warrant a new look at thermal-protection devices: Thermostats available in standard package styles make it easy to implement a temperature-control system right on your pc board.

—Anne Watson Swager, Associate Editor

A program guide for EISA vs MCA

75

Before developing new bus boards, manufacturers should consider the credentials of both IBM's Micro Channel Architecture (MCA) and the new contender in the add-in-board market—the Extended Industry Standard Architecture (EISA).—John Gallant, Associate Editor

Programmable logic: PLD architectures require scrutiny

91

When you look at high-gate-count programmable devices, whether PLDs or field-programmable gate arrays, you'll see a variety of architectures. To select the device that best suits your application, you must examine the strengths and weaknesses of each device.—Doug Conner, Regional Editor

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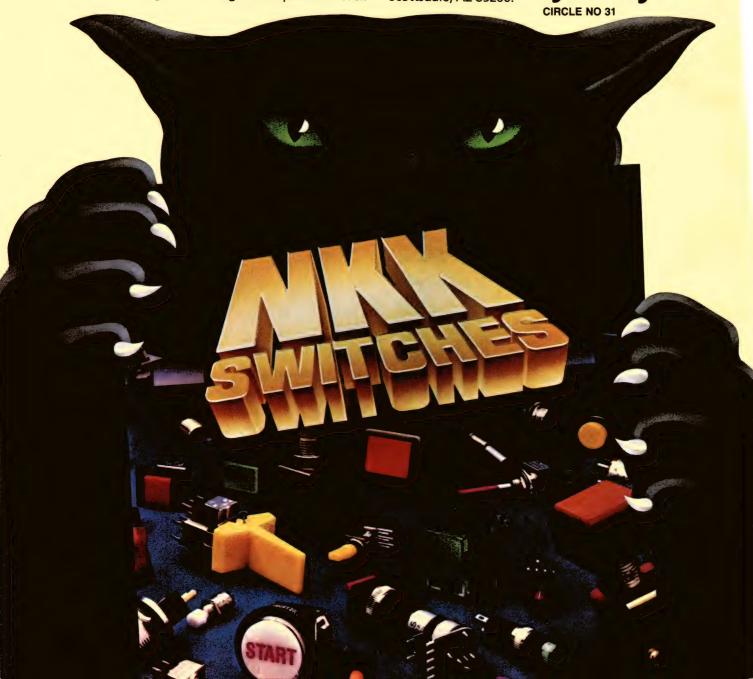
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EDITORIAL

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LOOKING AHEAD

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High performance boosts demand for op amps . . . US electronic shipments increase 5.3% from mid-1988.

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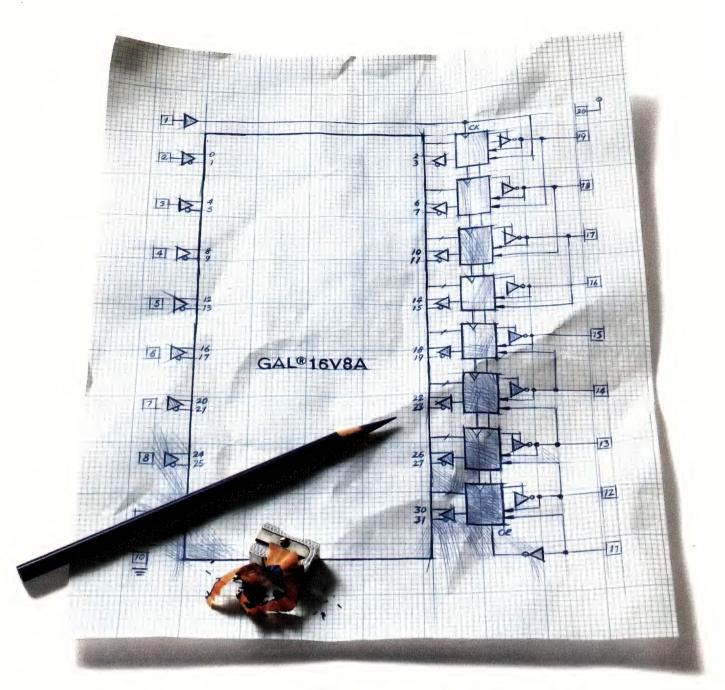


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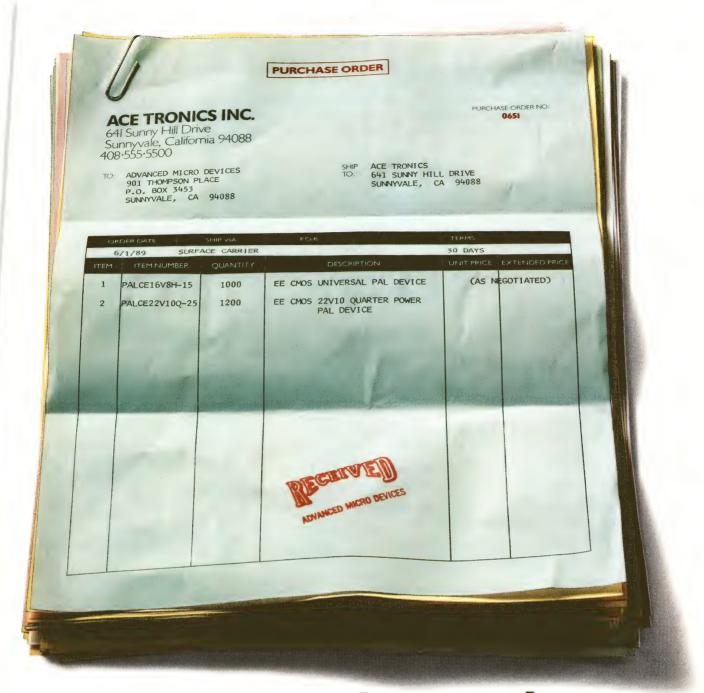


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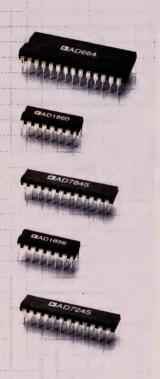
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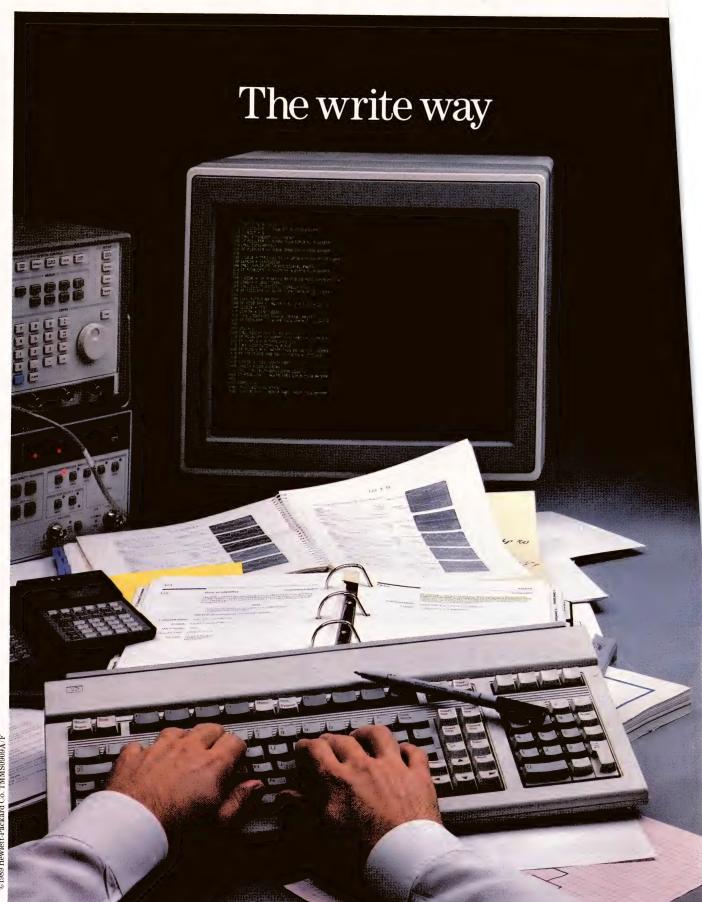
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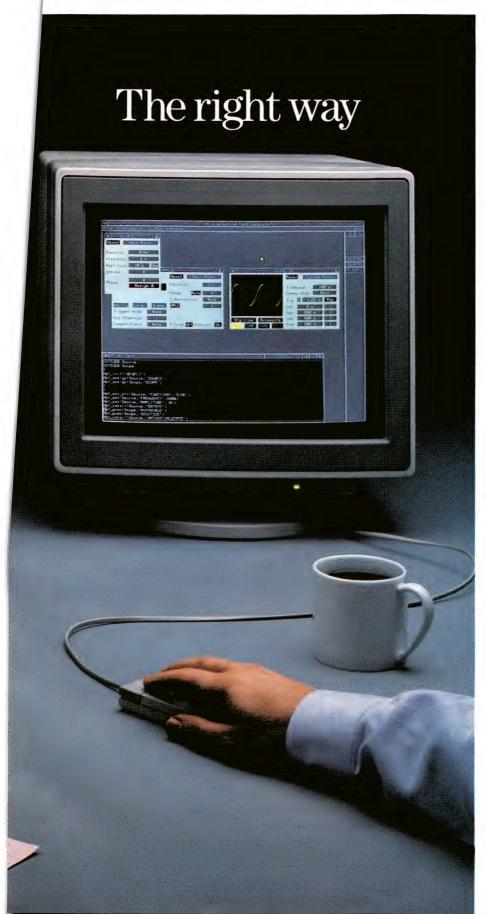
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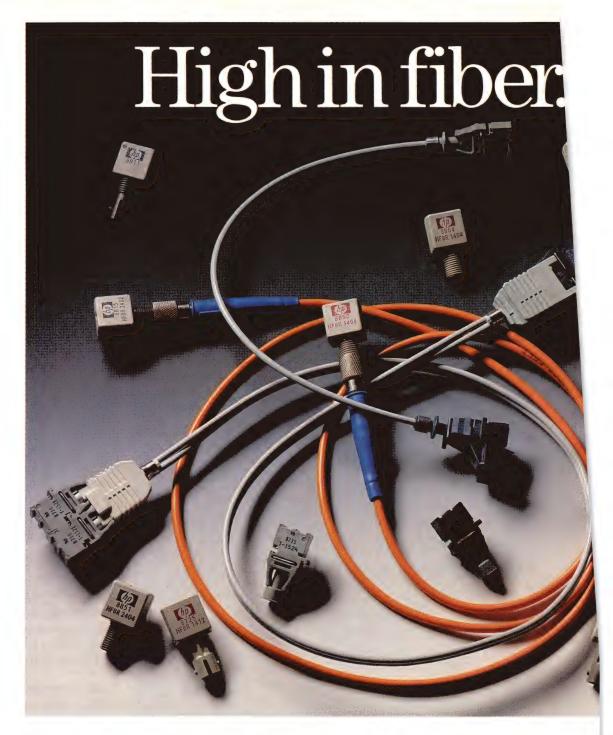
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CG 08905

NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

PC/AT-COMPATIBLE STD-BUS CPU BOARD OPERATES AT 20 MHz

The MCM286AT-20-2M STD-Bus CPU board from WinSystems Inc (Arlington, TX, (817) 274-7553) exceeds the performance of an IBM PS/2 Model 80 computer. Benchmarks yield a performance of 3793 Dhrystones. This board is hardware and software compatible with the IBM PC/AT and can run real-time executives, diagnostic software, and hardware-dependent programs developed for the PC/AT. The MCM286AT-20-20M contains as many as 2M bytes of parity RAM, 128k bytes of EPROM, two DMA channels, 15 interrupt channels, a battery-backed real-time clock, battery-backed configuration RAM, Phoenix BIOS, a speaker, a keyboard controller, two RS-232C channels, a Centronics printer port, a watchdog timer, and a reset switch. The \$1995 board operates as much as 23 times faster than a standard IBM PC/XT. To ensure compatibility with slower memory or I/O boards, the MCM286AT-20-M automatically switches speeds when accessing the STD Bus.—J D Mosley

HIGH-ACCURACY FREQUENCY STANDARD LOCKS TO LORAN

The FS700 loran-C frequency standard from Stanford Research Systems (Sunnyvale, CA, (408) 744-9040) delivers 10^{-12} long-term frequency stability and 10^{-10} (optionally 10^{-11}) short-term stability for \$4950. The unit operates by locking the frequency of its internal, 10-MHz, oven-stabilized crystal oscillator to the highly accurate cesium-clock-controlled loran-C transmitter pulses. The FS700 provides four 10-MHz outputs for use as time-base inputs to other instruments and a divided output in a 1-2-5 sequence from 0.01 Hz to 10 MHz. An internal phase detector lets you compare the divided output with an external signal for calibration of external sources. A remote active whip antenna included with the unit receives the loran-C signal.—Doug Conner

33-MHz RISC CHIPS AVAILABLE IN SAMPLES

Motorola's Microprocessor Products Group (Austin, TX, (512) 891-2839) is now sampling the 33-MHz versions of the 88000 microprocessor. The higher-speed processors, produced using 1.2-µm technology, follow the earlier 20- and 25-MHz versions and are rated at 28 MIPS. According to Motorola, the chips achieved benchmark performance of 64,500 Dhrystones and 33M single-precision Whetstones. The sample price for the 33-MHz 88100 CPU is \$894; the 33-MHz 88200 cache/memory-management unit costs \$1171. Delivery is 90 days ARO.—Michael C Markowitz

MODULE PROVIDES COMPLETE RISC CPU CORE

The IDT7RS101 from Integrated Device Technology (Santa Clara, CA, (408) 727-6116)) is a fully assembled and tested RISC CPU core on a 3.7×6.5-in. module. It comes in 12-, 16-, 20-, and 25-MHz speed grades and provides a way of incorporating RISC technology into your product without an extensive design effort. The module includes a 79R3000 processor, 64k bytes each of instruction and data cache, and address and data read and write buffers. A 79R3010 floating-point processor is available as an option.

To speed your RISC-based product's development, IDT is also offering the 79RS301 development board. This board accepts a 7RS101 module and adds to it a debug

EDN September 28, 1989

NEWS BREAKS

monitor program, 1M byte of SRAM, and two serial ports. You can use the development board to exercise the 7RS101 module or to test software development. The board costs \$3000; the modules cost \$1856 to \$3396 (100), depending on their speed specification.—Richard A Quinnell

SOFTWARE LETS YOU CONNECT YOUR MAC II TO IBM'S SNA NETWORK

To simplify the task of data communications between your Macintosh II and your company's IBM AS/400 or System 36/38 mainframe, KMW Systems Corp (Austin, TX, (512) 338-3000) has developed ApLINK, a program that provides file-transfer and terminal-emulation capabilities. Your Macintosh needs an Apple Coax/Twinax board and Finder or Multifinder system software. ApLINK lets you open as many as seven simultaneous sessions and enables your Macintosh to emulate the functions of an IBM 5251 terminal. This capability lets you access data that is stored in the IBM PC and use it in Macintosh software programs such as spreadsheets or word processors. The program costs \$395.—J D Mosley

DIGITAL SAMPLING OSCILLOSCOPE HITS 34 GHz

The HP 54123T digital sampling oscilloscope from Hewlett-Packard (Palo Alto, CA, (800) 752-0900) raises the band-width ceiling for general-purpose digital sampling scopes from 20 to 34 GHz. The 4-channel scope comprises an HP 54120B mainframe and an HP 54123 test set. A built-in time-domain reflectometry unit lets you perform transmission line measurements. The \$34,800 instrument also has statistical analysis and histogram capability to help you make quantitative noise, jitter, and eyepattern measurements.—Doug Conner

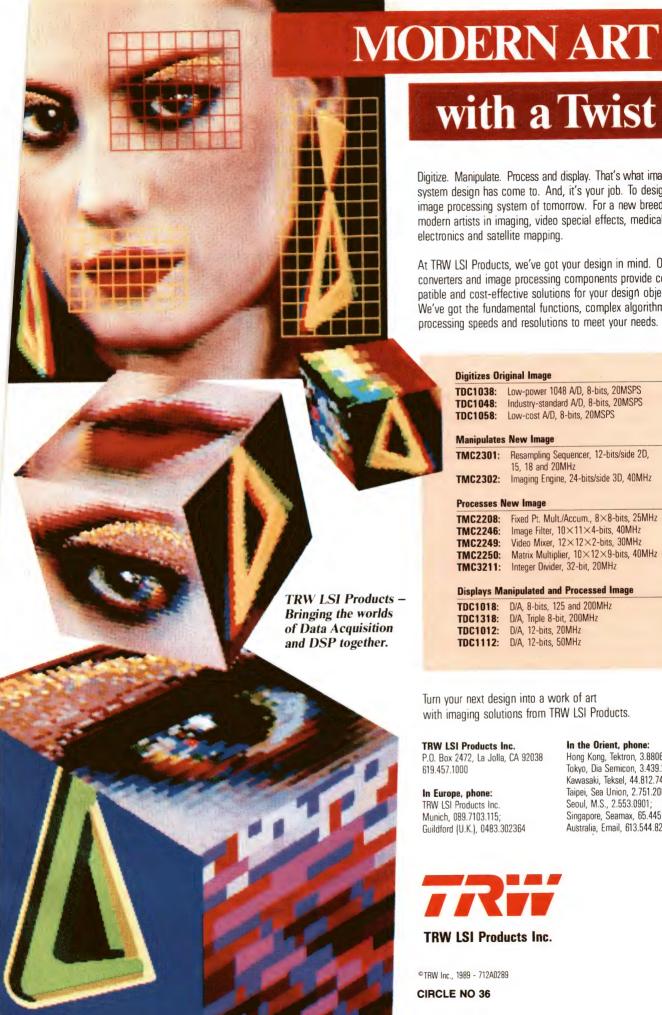
500M-BYTE HALF-HEIGHT DRIVE OFFERS 15-MHz TRANSFER

Selling for \$1560 (OEM), the Wren VI 5½-in., half-height, hard-disk drive from Imprimis (Minneapolis, MN, (612) 936-6271) uses zone-bit recording to provide a data-transfer rate of 15 to 21 MHz. This drive has an unformatted capacity of 502M bytes, an average seek time of 16 msec, and an MTBF rating of more than 40,000 hours. The unit comes with an embedded SCSI interface.—J D Mosley

CONTROLLER SIMPLIFIES HANDLING OF NONCACHEABLE MEMORY

Austek Microsystems' (Santa Clara, CA, (408) 988-8556) 386 cache controller, the A38202, includes logic that eases the use of cache memory in a system having coprocessors and memory-mapped I/O units. The device handles direct-mapped or 2-way set-associative caches of 32k to 128k bytes for CPU clock speeds as fast as 33 MHz.

The A38202's additional logic lets you define as many as three address ranges that are noncacheable. The controller passes any memory access in those ranges out to main memory. You can define a region to be noncacheable only for write operations, thus letting you cache PROM memory without altering the PROM image. The device also detects memory cycles intended for either the Intel 387 or Weitek 3167 coprocessor and disables cache during those cycles. It costs \$98 (10,000) and will be available in November.—Richard A Quinnell



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CIRCLE NO 36

NEWS BREAKS

CMOS SPARC PROCESSOR RUNS AT 40 MHz

Cypress Semiconductor has introduced a 40-MHz speed grade for its CY7C601 processor. The processor implements the SPARC 32-bit architecture. It has a 4-stage pipeline, 136 general-purpose registers, and a 32-bit virtual address space. It is fabricated in 0.8-µm CMOS, comes in a 207-pin PGA, and costs \$895 (100).

—Richard A Quinnell

PROGRAMMABLE DIGITAL I/O MODULE RIDES THE VXI BUS

The \$1995 73A-412 digital I/O module from Colorado Data Systems (Englewood, CO, (303) 762-1640) plugs into the VXIbus and provides 80 bidirectional, digital I/O lines. The 80 lines are organized as 10 8-bit ports, and you can configure each port as an input or output. The ports communicate with external devices by using a 2-wire handshake and a 3-state enable pin. Each of the TTL- and CMOS-compatible digital I/O lines can sink 24 mA.—Steven H Leibson

FDDI NODE CONTROLLER OFFERS 100M-BYTE/SEC DATA RATE

The V/FDDI 3211 node controller from Interphase Corp (Dallas, TX, (214) 350-9000) lets you connect your VMEbus-based computer system to a Fiber Distributed Data Interface (FDDI) fiber-optic LAN. Packaged on a double-height 6U VME board, the \$8000 V/FDDI 3211 contains 64k bytes of 32-bit-wide, 70-nsec, dual-ported RAM and is capable of transferring data at 100M bytes/sec. A RAM buffer controller and DMA chip manage onboard data transfers. You can configure two 3211s for some degree of fault-tolerant operation.—J D Mosley

KIT EASES EVALUATION OF HIGH-SPEED, 3-STATE PIN DRIVER

The EV-403A/B evaluation kit from Pulse Engineering (Torrance, CA, (213) 515-5330) lets you check out the characteristics of the company's 100-MHz PT-403 3-state pin driver. The EV-403A has one driver; the EV-403B has two. The EV-403B splits the input signal into a pair of nearly identical 50Ω outputs with output-high levels adjustable to greater than 4V into 50Ω or 8V into 1 M Ω . The EV-403B outputs' edge skew is 500 psec typ. You can set the output levels to a common value with ± 50 -mV resolution ($\pm 3\%$). Prices for the evaluation kit start at \$145; the PT-403 is \$36.25 (1000).—Margery Conner

REAL-TIME FRAME GRABBER PROVIDES 40-MHz SAMPLING RATES

Capable of capturing images from both analog and digital sources, the HI*DEF Display System from Imagraph (Chelmsford, MA, (508) 256-4624) plugs into your IBM PC/AT or compatible computer and displays data at sampling rates reaching 40 MHz. Using separate boards for frame grabbing and display buffering, the HI*DEF system provides a 1280×1024×8-pixel resolution with a palette of 16.7-million colors and an optional 2-bit overlay. An alternating-buffer scheme permits real-time capture and simultaneous display without producing scan lines on your monitor's display. The 2-board set sells for \$6995. With a daughter board that provides 4-channel analog frame grabbing, the set sells for \$8995. You can order the frame-grabber board alone for \$3495.—J D Mosley

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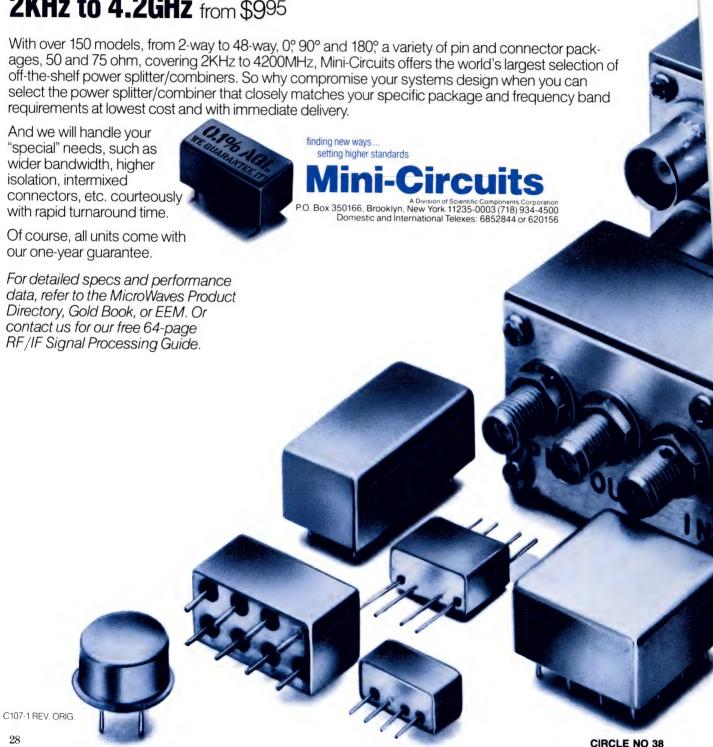
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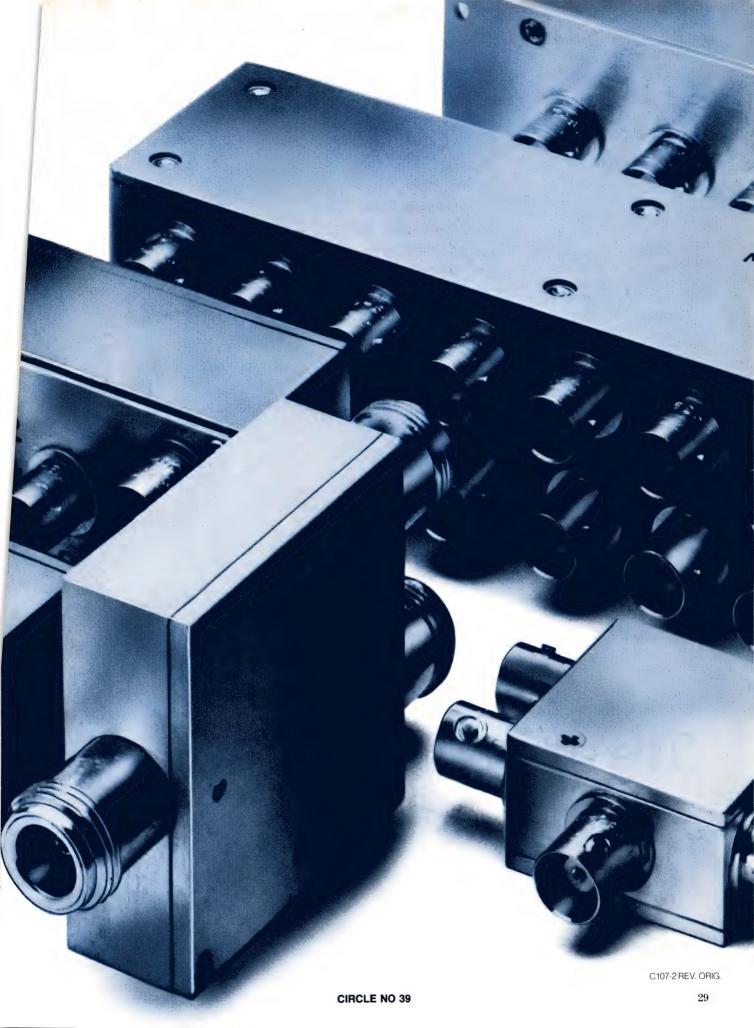
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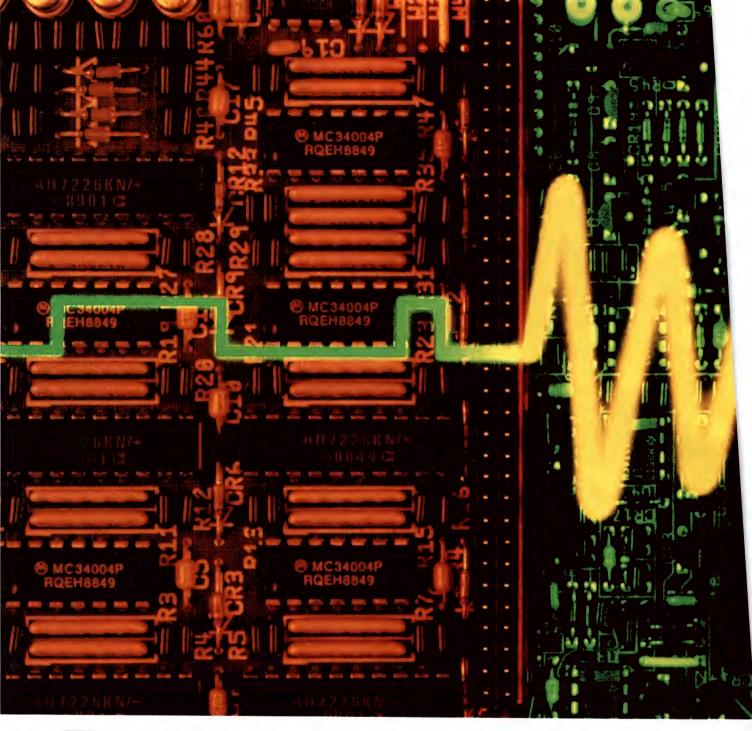


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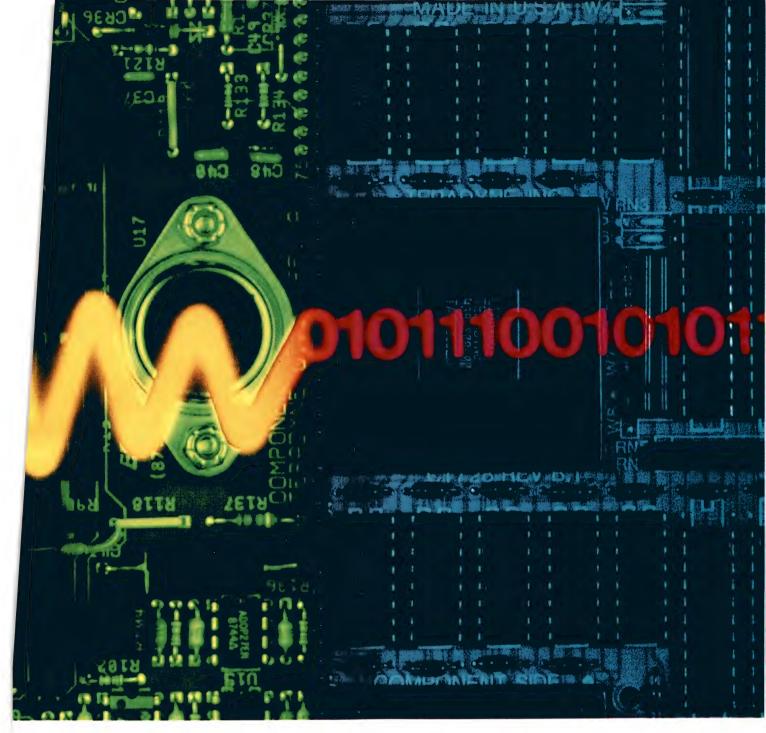


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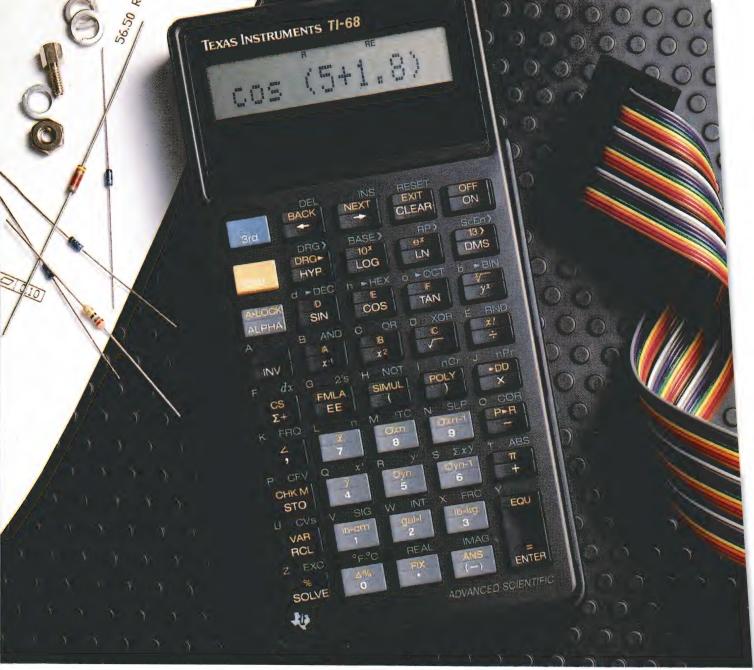
advanced products to market more efficiently.

With brain power like this, even difficult test problems become easy to solve. You'll start testing fast with low operating costs and highest circuit board yields at system assembly.

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about the new L350 VLSI Board Test System.





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rectangular forms for entries and results.

It also lets you easily check your equations with a 12-character alphanumeric display that can scroll through up to 80 characters for long equations. And, the last equation replay feature lets you edit or check the last computation without having to go back and reenter it.

In addition, when you need to solve quadratic, cubic or quartic equations, the TI-68's polynomial root finder will calculate the real and complex roots — automatically.

Working with number bases and conversions are also no problem. Perform arithmetic functions in decimal, hexadecimal, octal or

binary. And it does Boolean logic operations, too.

The TI-68 provides up to 440 program steps for as many as 12 user-generated formulas. It even stores up to 36 values in memories with user-defined alphanumeric names.

The TI-68 has what you've been looking for — the right functionality at the right price. See and try it at a nearby retailer, or call 1-806-747-1882 for additional information and to request free product literature.



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SIGNALS & NOISE

Looks almost like the filter chip he wants

A few companies are getting close to producing the filter chip I want. Sierra Semiconductor has the SC22324 eighth-order switched-capacitor filter that holds the filter parameters in EEPROM. That data is clocked in serially, then saved to EEPROM.

Linear Technology has the LTC1064 quad switched capacitor, but it uses external resistors. Maxim has the MAX 260 series dual universal second-order switched-capacitor filter that can hang on a processor bus; this feature is great if you have a processor, and your filter needs to be tunable. Finally, Xicor has the EEPot, a potentiometer that is set by a serial EEPROM.

What I'd like to see is a universal filter (could be pure analog or switched capacitor) that is tuned with an on-chip EPROM. The use of pure analog, instead of switched capacitor, allows the chip to work without a clock, further simplifying the outside circuitry. A typical active bandpass filter consists of an op amp, two capacitors, and three resistors. If we make the capacitors fixed and allow each of the resistors to be adjusted, using 1 or 2 bytes of the EPROM, we'd need 6 bytes of storage per filter.

To make programming easy, the chip should look like an EPROM when the V_{pp} pin is brought up to a high voltage of 12.5 to 25V. If a 24-pin package is used, the chip could emulate a 2732 during programming, allowing thousands of existing programmers to be used. When V_{pp} is removed, the chip looks like a bunch of filters. Again, with a 24-pin package, we could put at least 10 filters in the package, giv-

ing each its own input and output pins.

Is such a chip possible? Would anyone besides me buy them? I'll look forward to hearing responses from other EDN readers.

Harold Hallikainen Hallikainen & Friends San Luis Obispo, CA

Network provides access to global technologies

We read, with great interest, Jon Titus's editorial, "Coordinate science and technology R&D," (EDN, March 2, 1989, pg 45). As a part of NASA's outreach program to help American industry gain access to valuable global technologies, NERAC is a leader in technology transfer. The company was founded in 1966 to provide American industry access to technical and business



SIGNALS & NOISE

information drawn from NASA and other governmental agencies, as well as professional and academic organizations.

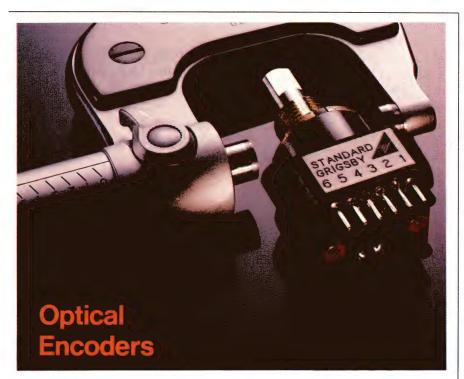
Our resources include databases in chemistry, electronics, metallurgy, engineering, patents, life sciences, marketing and management, and many others. Among our US governmental databases is the Fedrip database, a product of the Department of Commerce, which profiles Federal Research in Progress. Although Fedrip doesn't completely resolve the problem you highlight in your editorial, it does provide businesses an in-depth view of research activities conducted with

taxpayer monies.

Based in Tolland, CT, with a net work of representatives nationwide, NERAC provides technology assistance to a [variety] of businesses, large and small. Participants work with NERAC's staff of skilled technical experts to investigate information germane to their needs or problems, drawing upon NERAC's vast store of databases and federal liaisons as resources. Retrieved information may be in the form of a retrospective review of relevant published reports and papers, or a periodic update of the latest developments in a given

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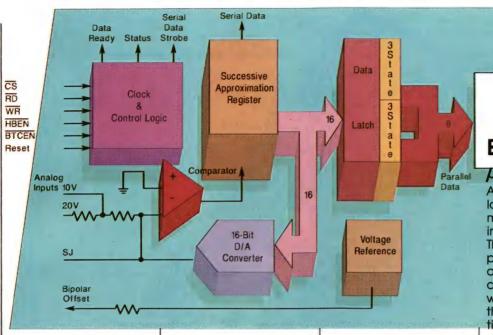
CIRCLE NO 2

Parallel problems in AM stereo and HDTV

Three cheers for your editorial on HDTV (EDN, July 20, 1989, pg 53). Ten years ago you published my letter predicting the demise of AM stereo because it did not address AM radio's main problem, program content. Today, TV has the same program-content problem. Flash and trash news, advertisements containing obvious lies of omission, and entertainment programs that have overused plot formulas and stereotyped characters will be just as offensive and boring in high resolution as they are now in low resolution.

James Long Sunnyvale, CA **INTRODUCING ADC700**

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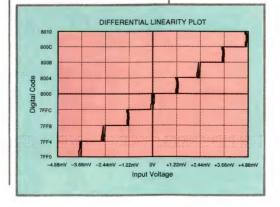
ADC700 comes complete with 16-bit A/D converter, laser-trimmed reference, clock, and 8-bit port microprocessor interface, all in a space-saving 28-pin hermetic ceramic DIP. Never before has a 16-bit ADC offered so much for so little.

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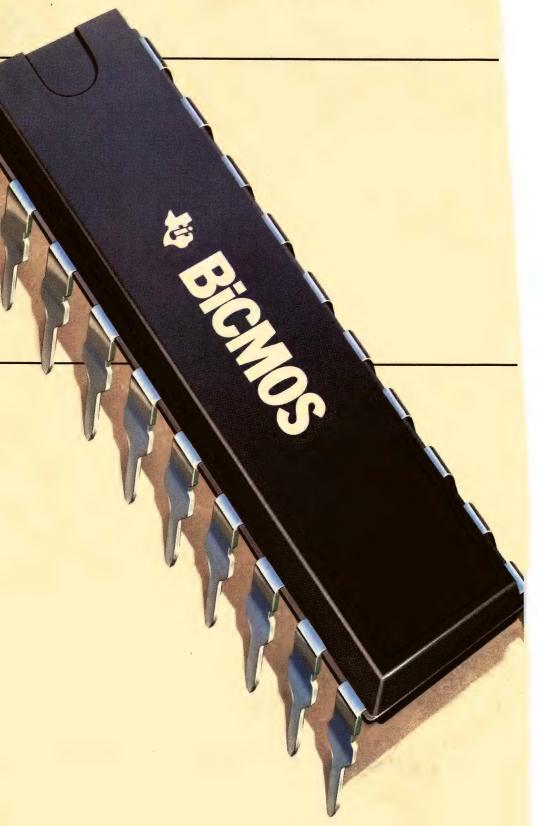
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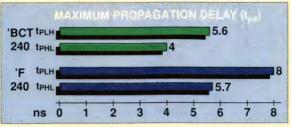
THE DOWN SIDE.



3iCMOS LOGIC

TI's BiCMOS logic gives you drive and speed up to par with advanced bipolar devices.

The chart says it all. Switching speeds of our BiCMOS family, designed specifically for bus interface implementations, are



TI's speed advantage: In a one-on-one comparison, a TI '74BCT240 BiCMOS octal bus driver proves to be much faster than a standard advanced bipolar equivalent.

comparable to advanced bipolar counterparts. Drive currents meet the requirements of today's industry-standard buses: 48/64 mA commercial, 24/48 mA military.

For example, our BCT2XXX memory drivers are two times faster than the competition's memory drivers. They not

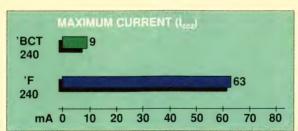
> only solve the undershoot/overshoot problems associated with driving DRAM memories but also conserve real estate by incorporating a 25ohm series damping resistor on chip.

With this speedy family comes a bonus, reduced switching noise. Case in point: An independent analysis* found our SN74BCT240 octal bus driver to have the fastest propagation delay (3.8-ns t_{PHI}) with the highest signal integrity (0.8-V simultaneous switching noise).

But there's another impressive side to the BiCMOS family story. Read on.

TI's BiCMOS logic cuts power consumption down to CMOS levels.

As you've gathered by now, our BiCMOS logic combines high-speed bipolar with low-power CMOS. Disabled currents can



TI's power advantage: Here again, the BiCMOS driver wins over the advanced bipolar counterpart, exhibiting far less power dissipation.

be reduced as much as 95% (see chart) while active currents are cut as much as 50% compared to advanced bipolar equivalents.

As a matter of fact, total system power savings can be more than 25%.

Our BiCMOS family now numbers more than 40 members and will top 90. All

members are compatible with advanced bipolar sockets, allowing easy plug-in upgrades.

BiCMOS technology is also enabling us to solve other problems that crop up in bus interface design. For example, the family will soon include a series of SCOPE™ Octals to provide system-embedded test capability. Also, the forthcoming BCT25XXX IWS line drivers will assure incident wave switching (IWS) down to 25 ohms.

For free samples of our BiCMOS logic family: In Europe call 44-234-223000, fax 44-234-223459, or write Customer Response Centre, MS 09, Texas Instruments Limited, Manton Lane, Bedford MK41 7PA, England. In Asia call 852-3-7351223, fax 852-3-7354954, or write Texas Instruments Hong Kong Limited, Market Communications Manager, 8/F World Shipping Centre, 7 Canton Road, Tsimshatsui, Hong Kong.

* David Shear, "EDN's advanced CMOS logic ground-bounce tests," EDN, Special Report, March 2, 1989.

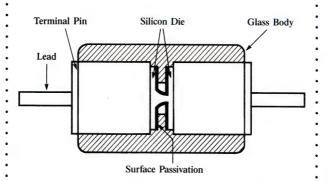
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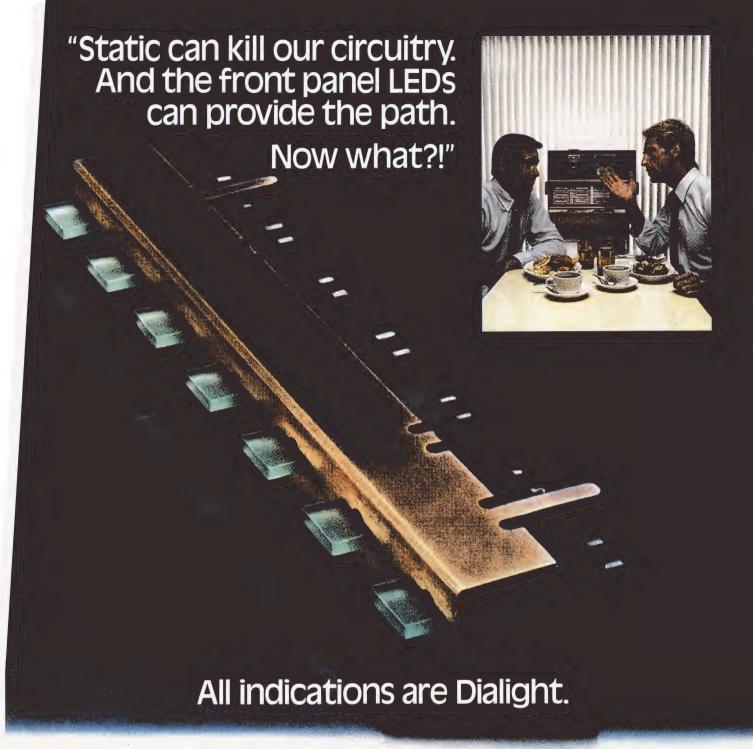
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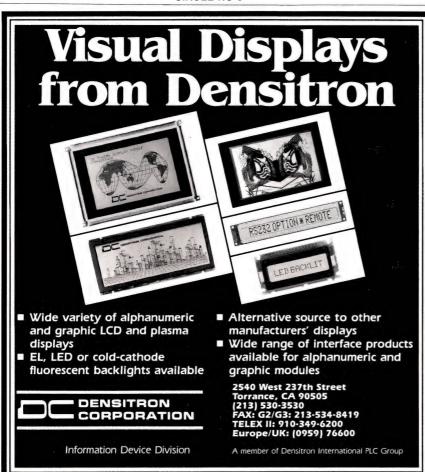
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CIRCLE NO 3



CALENDAR

IEEE International Conference on Computer Design (ICCD '89), Cambridge, MA. Giovanni De Micheli, Center for Integrated Systems, Room 129, Stanford University, Stanford, CA 94305. (415) 725-3632. October 2 to 4.

Electronic Imaging Conference East, Boston MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 2 to 5.

20th Korea Electronics Show, Seoul, Korea. Joseph Burke, US Department of Commerce, Washington, DC 20230. (202) 377-5014. October 7 to 12.

Policy and Parity: The Future of US-Japan High Technology Trade Policy (symposium), Boston, MA. Janet Fannon, Clearpoint Research Corp, 99 South St, Hopkinton, MA 01748. (617) 435-2301. October 12 to 14.

SECS Communications Seminar, San Jose, CA. GW Associates Inc, 1183 Bordeaux Dr, Suite 27, Sunnyvale, CA 94089. (408) 745-1844. FAX 408-745-6395. October 13.

Systems 89, Munich, West Germany. Gerald G Kallman, Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. FAX 201-652-3898. October 16 to 20.

Northcon/89, Portland, OR. Northcon/89, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. October 17 to 19.

Scan-Tech '89, San Jose, CA. Jane Yallum, AIM USA, 1326 Freeport Rd, Pittsburgh, PA 15238. (800) 338-0206. FAX 412-963-8753. October 17 to 19.

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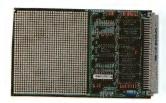


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CIRCLE NO 45



CIRCLE NO 5

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CALENDAR

Supercomputing World, San Francisco, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 17 to 20.

Digital Signal Processing, Single-Chip DSP Processors, Development Systems—Theory, Design and Applications, Munich, West Germany, October 23 to 26; in London, UK, October 30 to November 2. In the US, Dr Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. FAX 617-969-6689. In Europe, Andreas Kohl, Electronic Tools, Dusseldorf, West Germany. (49) 02102-841-013.

Unix Expo '89, New York, NY. National Expositions Co, 15 W 39th St, New York, NY 10018. (212) 391-9111. FAX 212-819-0755. November 1 to 3.

OEM Europe '89, Paris, France. Bureau International de Relations Publiques, Freddy J Rodriguez, 25 rue d'Astorg, 75008 Paris, France. (331) 47-42-20-21. FAX 331-47-42-75-68. November 7 to 10.

Productronica '89, Munich, West Germany. Gerald Kallman, Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. FAX 201-652-3898. November 7 to 11.

Wescon/89, San Francisco, CA. Wescon/89, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. FAX 213-641-5117. November 14 to 16.

VMEbus in Industry, Paris, France. VMEbus International Trade Association, Box 192, NL-5300 AD Zaltbommel, The Netherlands. 31-4180-14661. FAX 31-4180-15115. November 21 to 22.

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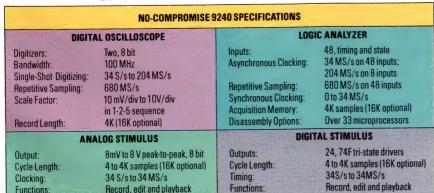
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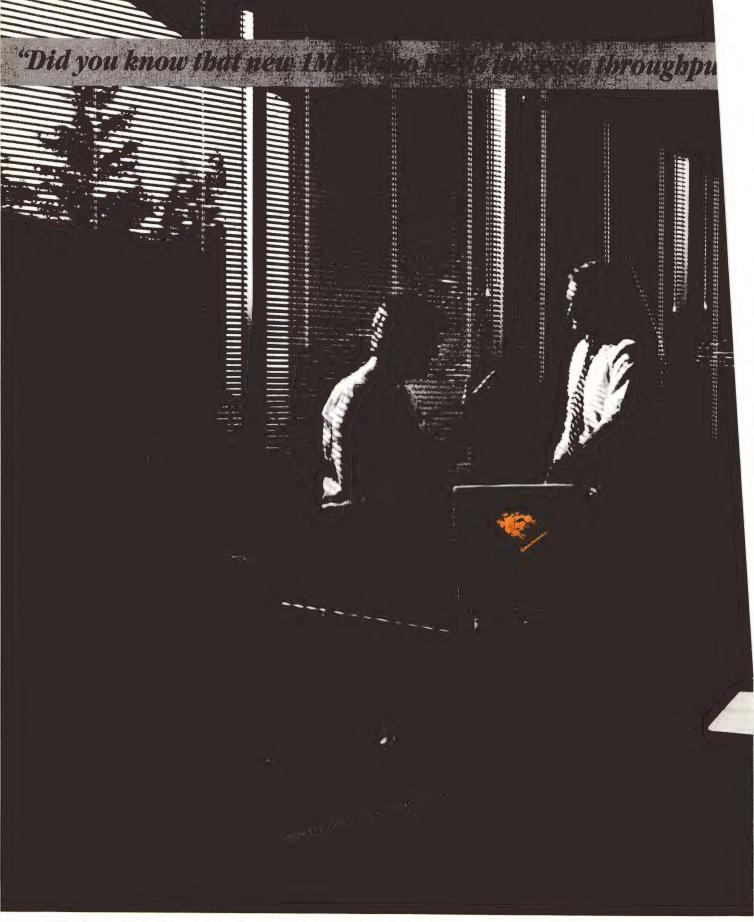




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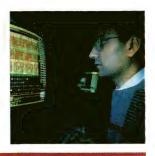
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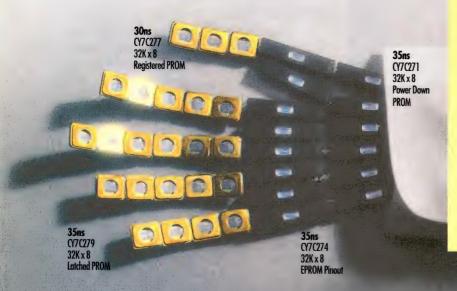
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EDITORIAL

Let's recognize bus leaders



We're pleased that the people who run the Buscon conferences are sponsoring an Outstanding Achievement Award. The award will recognize the one person who has had the most influence on the development of the computer-bus industry. EDN has helped nominate seven people for the award. The voting is up to you. Here are the nominees:

Lym Hevle is the Executive Director of the VME Industry Trade Association (VITA). Lym has been a champion of open buses and is active in pushing military-equipment suppliers to adopt open bus architectures.

Ray Alderman, Vice President of Matrix Corp, is a prominent bus-industry spokesman. Ray has directed the International Board-Level Symposium since it started, and he recently finished a detailed study of the computer-bus industry.

Shlomo Pri-Tal, who works at Motorola, is one of the founding fathers of the VMEbus specification and an outspoken supporter of bus standardization. He's also chairman of the Next Generation Architecture (NGA) technical committee.

Wayne Fischer is the marketing director at Force Computers. He was one of the authors of the VMEbus specification and is a proponent of the Futurebus+ architecture.

Paul Borrill is the chairman of the IEEE's Futurebus + committee. He played an important role in developing the Multibus II specification, and he has been very active in the standards committees for the popular open buses.

Jim Ready of Ready Systems is a pioneer in putting together software development tools for real-time-software developers. He has served on many open-bus committees and advocates using Ada for real-time applications.

John Hyde, who works at Intel, is a leading spokesperson for the Multibus II architecture. John is a proponent of the Futurebus+ standard, and he has been working to foster cooperation between the Multibus Manufacturers' Group (MMG) and VITA as each group defines future buses.

The sketches above are necessarily brief, but each person listed is deserving of the award. It's unfortunate that there's only one award. Now it's time for you to vote; the deadline is January 15, 1990. You can send your written choice by mail or facsimile to

Conference Management Corp 200 Connecticut Ave Norwalk, CT 06856 FAX 203-838-3710.

Write-in votes are acceptable; send the name of your nominee and a description of his or her accomplishments. Write-in votes will also help us identify people who should be among next year's candidates. The recipient of the 1989 award will be announced during Buscon '90 West in Long Beach, CA this February.

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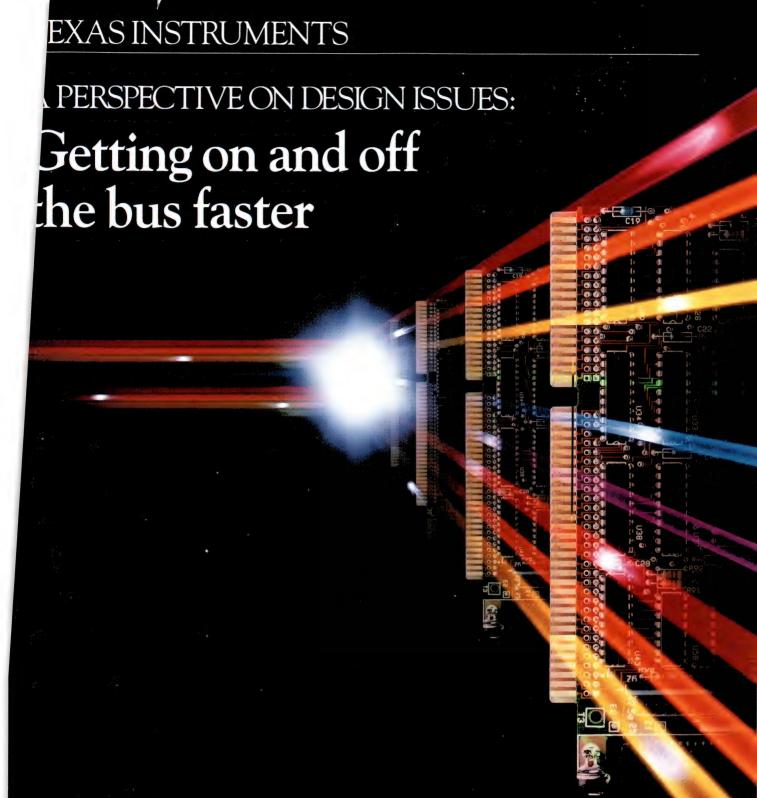
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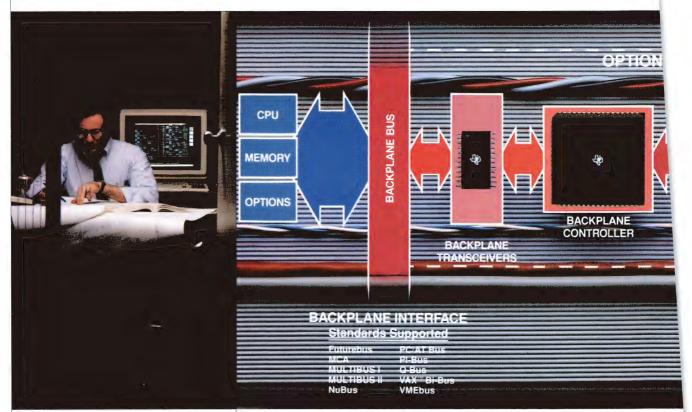
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hat use is a high-performance CPU if its processing power can't be delivered to the backplane and outward to the peripherals?

Typically, some system throughput is lost at the local bus interface, some at the backplane interface, and some at the peripheral bus interface.

To help you minimize such losses and maximize system throughput, Texas Instruments offers a series of innovative chips for (1) backplane interface and (2) peripheral bus interface, as well as (3) controllers to regulate data flow.

These devices support the major industry standards listed above so that you can achieve system compatibility regardless of the bus you are implementing.

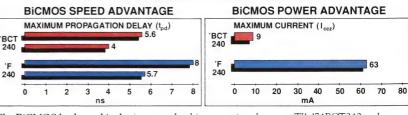
Superior backplane interface performance

To maximize system throughput, data must be able to get on and off the bus quickly. Therefore, the backplane bus transceivers must be capable of high speed and high drive.

Our high-speed/low-power BiCMOS logic (SN54/74BCTXXX) is specifically designed for bus interface applications.

As the name implies, TI BiCMOS merges low-power CMOS with high-speed bipolar, delivering switching speeds comparable to advanced bipolar devices. You also get the 48/64-mA

BICMOS VERSUS ADVANCED BIPOLAR



The BiCMOS lead over bipolar is proven by this comparison between TI's '74BCT240 and a comparable advanced bipolar standard device. Typical propagation delay of TI's BiCMOS part is faster (*left*) while power dissipation is less (*right*).



ICs. To complete the implementation, TI offers a series of innovative standard and ASIC control devices. Use of TI's leadership bus interface devices can help shorten system design cycles.

drive current you need, and total system power savings can be as high as 25% (see charts).

There are more than 60 members in our BiCMOS family, including 8-, 9-, and 10-bit latches, buffers, drivers, and transceivers. The family is also available in military versions.

Our family of octal ECL translators (SN10KHT/100KTXXXX) delivers a low-power, high-speed translator solution with 48 mA of

drive capability on the TTL side.

Our high-speed Futurebus transceiver family (SN55/75ALS-05X) includes quad and octal devices compatible with Futurebus implementations of the IEEE 896.1 standard. With a drive capability of 100 mA, a 5-ns (typ) propagation delay, and a supply current of 65 mA (max), our SN75ALS053 has the best speed/power ratio of any Futurebus transceiver on the market today.

High-performance peripheral interfaces

Peripheral bus interface design decisions revolve around trade-offs between line length, data rate, and noise immunity.

Where data rates are low and

line lengths are short, as with the popular RS-232-C/D standard, the major concern is power savings. However, relatively high voltages (30 V) prevent the use of standard

CMOS devices. Your answer lies with TI's Linear BiCMOS family.

Included are low-power versions of industry-standard quad drivers and receivers (SN75C188/89). Driver/receiver combinations, ranging from single to quad combinations (SN75C1154), substantially cut package count.

This BiCMOS technology will also allow us to provide charge pump circuitry for single 5-V operation.

Where data rates are high and line lengths are long, as the newer peripherals demand, noise can become a major problem. It is overcome by the use of differential drive. Typically, the major application requirement is higher speeds at, ideally, lower power.

For example, disk drives using ESDI, IPI, or SCSI interfaces will benefit from TI's SN75ALS17X devices conforming to RS-422-A and/or RS-485 standards. These chips are fabricated using our unique IMPACT™ processing that delivers up to 50% greater speed compared to competing products with as much as a 30% power reduction.

IMPACT processing is also behind the unmatched speed of our SN75AS030 RS-422 dual driver/ receiver. Typical propagation delays are only 6 ns. ■

No matter which of TI's innovative devices you choose to improve speed, cut power, and reduce real estate at the media interface, the complete bus interface requires another element — controllers. For details on how TI is addressing your needs in this area, turn the page.



High-performance controllers make system design easier.

While the majority of physicallayer devices—those used to implement backplane and peripheral interfaces—transmit data, your system design also requires a device to regulate the flow of that data through the bus interface. To do the job, TI offers a series of controllers that simplify and shorten your task while cutting chip count and improving overall system throughput.

Simplified NuBus design

TI has taken much of the work out of NuBus™ design by introducing the industry's first standard NuBus interface devices. They are the SN74ACT2440 NuBus Controller and the SN74BCT2420 NuBus Registered Transceiver.

A typical implementation, using two 16-bit transceivers and one 32-bit controller (see below), replaces as many as 45 discrete devices. Compared to a discrete approach, this solution uses 60% less board space and 90% less power.

Because the necessary logic is embedded within the controller, design cycle time is reduced significantly.

A low-power UART

There is now more need than ever for low-power RS-232 interfaces. Our TL16C450 Universal Asynchronous Receiver/Transceiver (UART), made with CMOS process technology, is an excellent choice for desktop applications and is especially suited for use in laptop/battery-powered units.

A flexible SCSI controller

Available soon, our SCSI controller (designed to conform to ANSI X3.131-1986 specifications) will deliver data rates of 3 Mbytes/s (asynchronous) and 5 Mbytes/s (synchronous).

Unique byte-stacking control logic will allow interface to 16, 24, and 32-bit buses. The TI controller will also provide powerful multiphase SCSI commands, including automatic handling of save-data pointer to minimize interrupts to the host processor. Dual 32-byte FIFOs will provide smooth, efficient buffering between processor and DMA ports.

Customized controllers, too

The NuBus and UART controllers

are available as part of our ASIC standard-cell library.

In addition, TI offers TGC100 Gate Arrays and TSC500 Standar Cells as part of our ASIC family which allows you to build the precise chip functions you need.

System complexity and the future

As systems become more and more complex, the need will emerge for combining the functionality of controllers and physical-layer devices on a single chip. To that end, TI is applying its acknowledged expertise in physical-layer devices to the design and development of such advanced control-level ICs.

System complexity also brings with it the need for simulation models to make design easier and faster. As a result, we already have simulation models available for more than 1,300 TI devices, including BiCMOS bus interface and ACL logic devices.

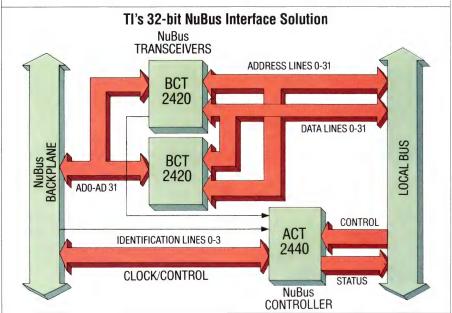
Another issue is the increasing difficulty and expense of testing boards in complex systems. Consequently, TI supports the JTAG/IEEE P1149.1 standard with the development of standard products and ASICs having on-chip test cells, as well as with development support software and device models on several leading workstations.

Please call 1-800-232-3200, ext. 3905, for your copy of our Bus Interface Devices brochure. Or write Texas Instruments Incorporated, Dept. SSY25, P.O. Box 809066, Dallas, Texas 75380-9066.

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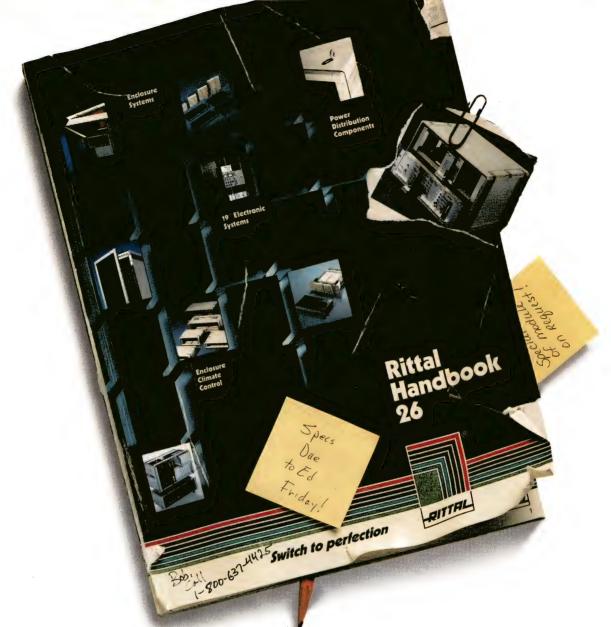
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Major space savings are realized by using one TI SN74ACT2440 controller and two SN74BCT2420 transceivers to complete a full 32-bit NuBus master/slave interface. As many as 45 discrete logic devices are replaced, realizing significant reductions in board space, power consumption, and design cycle time.





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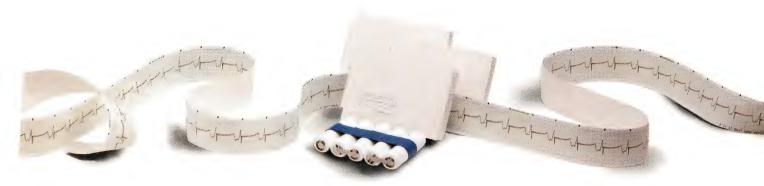
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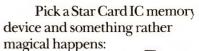
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TECHNOLOGY UPDATE

Thermostat packaging adds design flexibility



Today's thermostats are available in standard packages, so you can attach a thermostat to your pc board as easily as you can insert a transistor.

Anne Watson Swager, Associate Editor

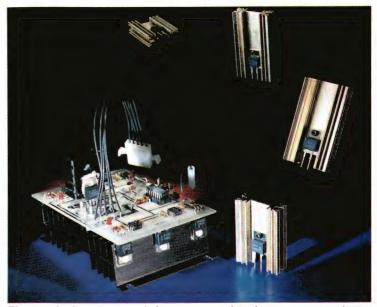
hermostats are now available in DIP, surface-mount DIP, TO-5, and TO-220 package styles, making it easy to implement a temperature-control or overtemperature-warning system right on a pc board. Thermostats in these standard configurations can sense pc-board ambient temperatures or monitor the surface temperature of a heat sink. Although these devices are based on a long-established, bimetaldisc technology, the higher density of transistors within ICs-and of surfacemount ICs on pc boards-warrants a new look at how thermostats can alert you to heat-related problems.

In addition to thermostats, you can choose from a variety of products for thermal protection, such as thermistors

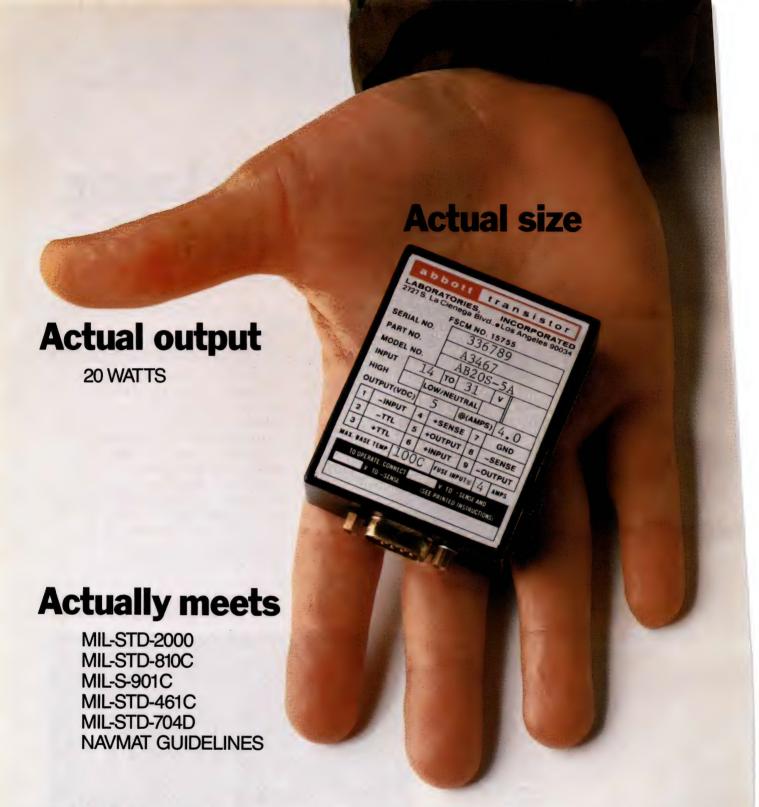
and thermal fuses. The usefulness of these devices is limited, however. Thermistors require external components to control temperature, and thermal fuses are simply shutdown mechanisms that require manual replacement. The thermostat is the most versatile thermal protector because it can both sense and act on temperature changes. It can also provide advance warning of temperatures beyond desired limits or shut down an entire system.

Motor protectors are specialized thermal protectors that include a thermostat along with an internal heating element. The internal heaters simulate the increased winding temperatures that are caused by an increase in current. The thermostat protects against excessive temperature, and the heaters protect against excessive current.

The basic thermostat is a disc-operated, bimetal thermal switch, typically spst or spdt. The contacts of these switches open and close at factory-preset temperatures based on the snap action of an internal bimetal disc. Although the action of each switch from each manufacturer varies somewhat, **Fig 1** illustrates their typical construc-



The standard packaging of thermostats makes them more convenient to use in many applications. The 6700 Series from Airpax conforms to the TO-220 package standard and can sense the surface temperature of heat sinks.



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TECHNOLOGY UPDATE

Thermostats

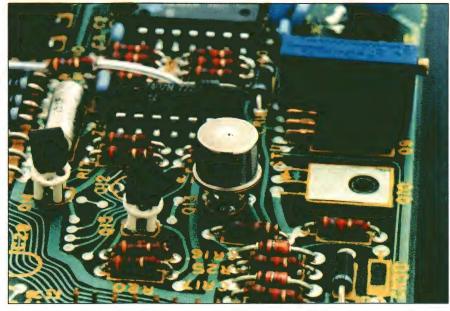
tion. The bimetal disc is a temperature-sensitive actuating element. As the temperature reaches its calibration point, the curvature of the internal disc snaps to its reverse position, which activates the switching mechanism. This mechanism in turn opens or closes the switch.

Switches are available that either open or close due to a temperature rise. Most switches reset automatically once the temperature decreases to a certain point, but manual-reset thermostats are also available. For example, Selco Products' Model 603, which sells for \$4 (100), features a pushbutton reset.

Packages add convenience

Each thermostat is a combination of physical, electrical, and thermal characteristics; these three properties determine which thermostat you choose. Thermostat manufacturers design newer devices with physical characteristics—namely packaging—in mind, offering familiar DIP, surface-mount DIP, TO-220, and TO-5 standard package styles. Before a few years ago, most thermostats were based on a 0.5-in., snap-action disk design, but these newer devices feature subminiature construction.

Airpax recently made its 6600 DIP Series of spst thermostats



Thermostats in TO-5 packages, such as Elmwood Sensors' 3600 Series, are designed to sense the ambient temperature on and around pc boards that are stuffed with logic-level circuitry.

available in a gull-wing, surface-mount package. Both the standard DIP and surface-mount devices are designed for use on pc boards. Typical uses include turning on an indicator light or audible alarm, switching on a control circuit, controlling the speed of a fan, or shutting down a system.

The company also manufactures the 6700 Series spst thermostats, which are housed in a TO-220 package. The 6700 Series was developed primarily for use with power supplies, power-conditioning equipment, and uninterruptible power supplies, but you can also use it on pc boards. The thermostat features a nickel-plated, copper mounting bracket isolated from the operating contacts. This mounting bracket lets you install the thermostat directly on a heat sink. By sensing the surface temperature, the thermostat detects any overtemperature condition caused by components that are mounted directly to the heat sink or in proximity to it. Both the 6600 and 6700 Series devices cost less than \$2 (10,000).

Thermal spst switches are available in a TO-5 package from Elmwood Sensors and Therm-O-Disc. Like Airpax's 6600 Series, these devices are designed to protect low-power and logic-level circuitry by monitoring ambient temperature around the pc board. Elmwood's 3600 opens on temperature rise, and the 3601 closes on temperature rise; both types cost less than \$2 (5000). The 83T thermal switches from Therm-O-Disc cost

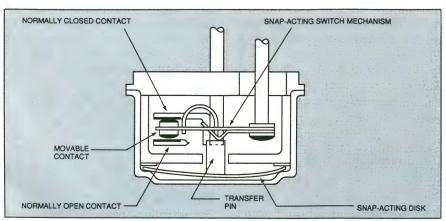


Fig 1—The operation of most thermostats is based on a snap-acting disk mechanism. As the temperature rises, the disk snaps to its reverse curvature position and activates the switch mechanism.

EDN September 28, 1989

TECHNOLOGY UPDATE

Thermostats

\$2.25 (5000).

All of these devices in standard packages are compatible with auto-insertion equipment and can withstand wave-soldering and board-washing operations. The TO-5 devices are hermetically sealed, and Elmwood's 3600 features an electrically isolated case ground lead.

Devices brave harsh environments

Other precision thermostats are packaged to withstand rugged environments. These devices include specifications for acceleration, shock resistance, and vibration resistance, and they meet MIL-S-24236. Both Texas Instruments and Elmwood Sensors provide thermostats for these environments, but not in standard electronic packages.

Texas Instruments' extensive line of Klixon products includes precision thermostats such as the 3BT and 4BT devices, which feature military qualification in a lightweight (0.2 to 0.9g), miniature-size (0.189×0.156-in.) package. A variety of packages are available, including packages with pin-type terminals for pc-board assembly. The 3BTs at \$7 (1000) and 4BTs at \$9 (1000) can withstand 100g of shock, 30g of vibration (5 to 2000 Hz), and 200g of acceleration.

TI's 5BT spdt thermostat (\$16 (1000)), one of few thermostats that has a double-throw contact, is a high-reliability, hermetically sealed thermal switch. You can use one pole of the switch to control a cooling fan and the other pole to signal another control element, such as a μ P. The diameter of the 5BT package is approximately 0.64 in., and its height is approximately 0.358 in.

Elmwood Sensors' 3200 and 3500 Series thermostats are designed for high-end military applications. These devices meet MIL-S-24236 and MIL-STD-1547 level S requirements, and they're qualified for use in space shuttles and other propul-



Thermal cutoffs implement one form of thermal protection. Thermo-O-Disc's Microtemp cutoffs, priced at \$0.30 (5000), open the circuit when overtemperature occurs and must be manually replaced. The photo also features the company's 36T thermostat.

sion vehicles. Specifically, you can use them in heat blankets, gyroscope temperature controls, and batteries. The 3500 Series features high reliability in extreme environments, which may be encountered in applications such as aircraft-wing temperature control. These sensors cost from \$20 to \$400 each and are usually made to order.

Check current, voltage ratings

Physical characteristics are important for ease of use, but the thermostat's electrical characteristics are critical to its performance. The current and voltage ratings must be sufficient for your application. You must also consider the amount of contact isolation and the contact resistance.

Another important characteristic is the time required for the switch contacts to make and break. Unfortunately, many thermostat data sheets don't specify the switch time. According to TI, the switch time also depends on aspects around the thermostat such as the mounting surface and the air veloc-

ity. Switch time is therefore difficult to specify. The company says that its 3BT and 4BT devices switch in less than 5 sec under most conditions. As for the thermostats in standard packages, Airpax does specify the contact bounce-to-make time for its 6600 and 6700 Series as 3 msec max.

The electrical ratings for the small, pc-board-mountable packages lie roughly in the same range and apply only to resistive loads. The contact resistance of the devices typically ranges from 20 to 50 $m\Omega$. The insulation resistance at 500V dc varies from 20 M Ω for Elmwood's 3600 to 100 M Ω for the Airpax models. Airpax's 6600 and 6700 Series have contact ratings of 30,000 cycles at 1A, 48V dc or 100,000 cycles at 20mA, 5V dc; Elmwood's 3600 is rated at 1A, 28V dc/ac and at 5mA, 5V dc/ac for 100,000 cycles. The 83T from Therm-O-Disc has contact ratings of 1A, 35V dc for 10,000 cycles and 1mA, 10mV dc for 100,000 cycles.

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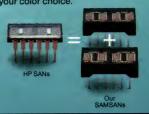
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TECHNOLOGY UPDATE

Thermostats

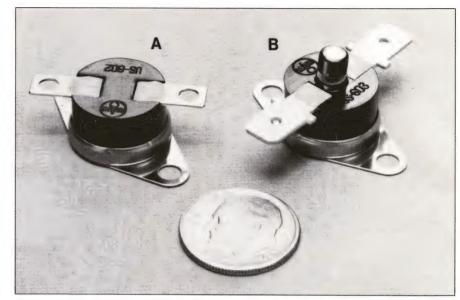
slightly higher ratings. For example, Elmwood's 3200 Series for aerospace and military applications are rated at 5A, 28V dc resistive load. The 3500 devices are rated at 5A, 30V dc or 115V ac resistive load. All ratings are for 100,000 cycles of operation. The company also rates these military products for inductive and lamp loads.

Choose the switch point

The last set of specifications you should consider before choosing a thermostat are its thermal characteristics. These characteristics include the device's operating temperature range, the temperatures at which the contacts open and close, and the differential temperature that allows the thermostat to return to its original position once the temperature returns to a safe level. The specifications usually include a typical open (or close) temperature and a minimum close (or open) temperature, with a minimum specification for the differential between the two.

Most of the thermostats mentioned belong to families that include preset values in degree increments. Thermostats in DIP, TO-5, and TO-220 packages typically feature temperature trip points from 40 to 120°C in 5-degree increments. The differential temperatures range from 4 to 9°C.

High-reliability and military devices feature wider temperature ranges. Elmwood's 3200 and 3500 Series include devices with trip points from -51 to +163°C and -51 to +204°C, respectively. TI's 5BTs feature trip points from -65 to +450°F (-54 to +232°C). The differential temperature ranges for these devices vary. Elmwood's 3200 and 3500 Series feature devices whose differentials range from 9 to 20°C and 5 to 40°C, respectively. The standard differential for TI's 5BTs is between 20 and 30°F (ap-



Pushbutton reset thermostats are available from Selco Products. Their 602 and 603 autoand manual-reset, spst thermostatic switches feature temperature set points from 60 to 450°F (15 to 232°C).

proximately 11 to 16°C).

When you're comparing the physical, electrical, and thermal characteristics of these thermostats, remember that thermostat manufacturers offer many custom products, and most of the manufacturers mentioned here have custom-development capabilities. Custom products are much costlier than off-the-shelf devices, but if you need

a combination of features that aren't available in one product, you probably can get them custom made. Fortunately, manufacturers currently offer standard products in packages that suit many electronics applications.

Article Interest Quotient (Circle One) High 515 Medium 516 Low 517

For more information . . .

For more information on the thermostats discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

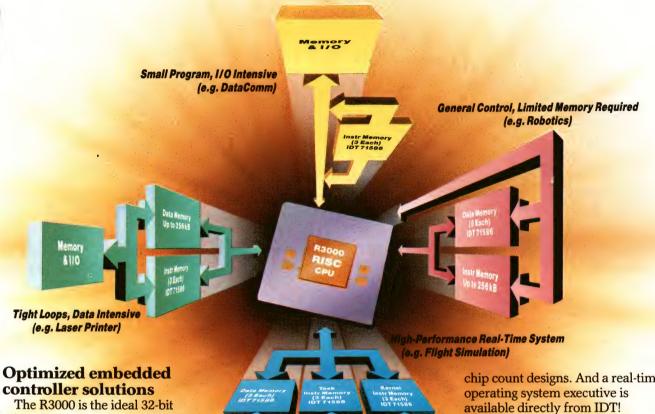
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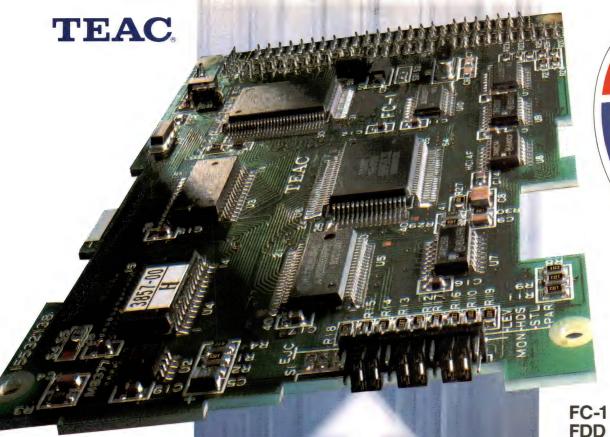
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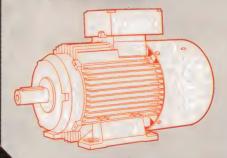


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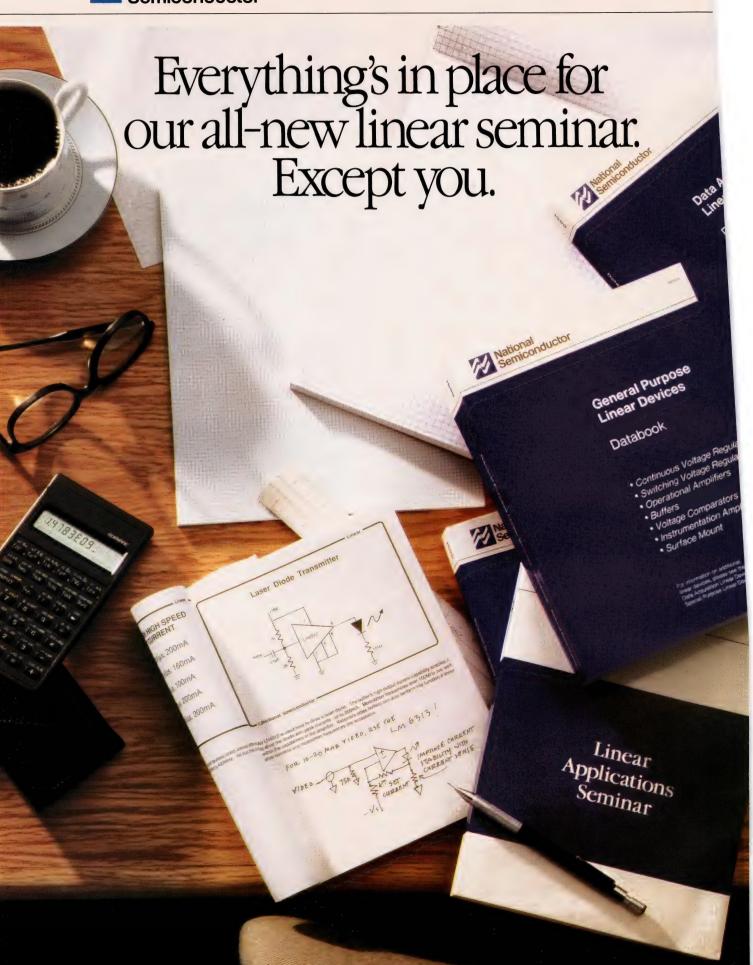
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A program guide for EISA vs MCA



The introduction of EISA interface ICs indicates that the EISA vs MCA bus fight is about to begin. You should compare the credentials of each contender before betting on a winner.

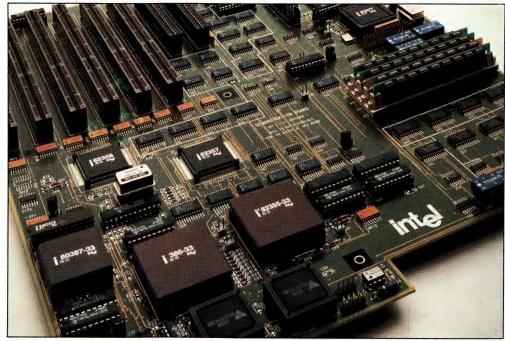
John Gallant, Associate Editor

he introduction of computers for the Extended Industry Standard Architecture (EISA) in the fourth quarter of this year opens up new opportunities for add-in-board manufacturers. In fact, a dominance battle may be brewing in the early 1990s between this upstart bus structure and its slightly more mature rival, IBM's Micro Channel Architecture (MCA), which was introduced in April 1987. Whether the battle will produce a clear-cut champion is uncertain, but board manufacturers should compare the "tale of the tape" for the two contenders before developing new boards for either bus.

Both EISA and MCA enhance the

performance of IBM's 16-bit PC/AT bus, now known as the Industry Standard Architecture, or ISA (pronounced eyesah). The architectures reflect the increased capabilities designed into Intel's 32-bit- μ P family—beginning with the 80386 μ P and extending to future family members such as the 80486. Therefore, it isn't surprising that the EISA (pronounced ee-sah) bus and the MCA bus have many similarities.

The two architectures feature programmable-configuration registers that eliminate the need for DIP switches, which are common to the ISA architecture. In addition, both systems define separate 32-bit address and 32-bit data buses along with control signals that are



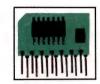
EISA's maiden voyage into the PC arena begins with the availability of Intel's 82350 EISA chip set and the MCS automatic-configuration utility.

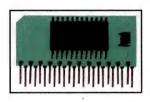
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EISA vs MCA

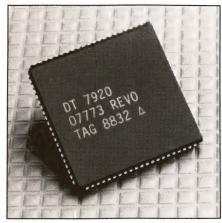
compatible with Intel's 32-bit μP family. Both architectures also define a bus-arbitration protocol when multiple DMA slaves and bus masters coexist with the CPU. Further, unlike the ISA bus, both EISA and MCA implement an improved power and ground system to handle higher-speed technologies. In addition, they implement shared, level-sensitive interrupts to improve the reliability of the interrupt system.

Different strokes

The differences between the two architectures are primarily in design philosophy. MCA is a result of an internal collaboration between IBM's PC and mainframe organizations. In designing the MCA, the company took a revolutionary approach to bus structure, believing that defining a new bus architecture would be more efficient than implementing the design changes into the ISA.

In contrast, the consortium of nine computer manufacturers who defined EISA were driven by other ambitions. The so-called "gang-ofnine"—Compag, Epson, AST, Hewlett-Packard, NEC, Olivetti, Tandy, Wyse, and Zenith-wants to remove itself from under IBM's umbrella by developing an open architecture that won't be held hostage to specification changes, which IBM could introduce at any time. In addition, the consortium believes that a wide customer base exists for an advanced, 32-bit bus architecture that's backward compatible with ISA-style plug-in boards.

You only have to see the differences between the bus connectors to observe the differences in the design philosophies of the two buses. The timing requirements of high-performance µPs, such as Intel's 80386, would strain ISA's conformance to electromagnetic radiation standards. Therefore, IBM uses a more effective distributed-power



Board-interface ICs proliferate for IBM's PS/2 MCA computer bus. Data Translation's DT7920 has two independent DMA controllers that can arbitrate for bus control. The configuration lets you bandy data between two DMA channels for largely uninterrupted data transfer.

and -ground system throughout the MCA bus connector to contain emitted radio frequencies.

An ac ground is on every fourth pin on both sides of the MCA bus connector. The ground pins on one side of the connector are offset by two pins from the ground pins on the other side. In addition, the connector uses pins spaced 50 mils apart, as in the lead spacing of many surface-mount components. The signal-pin organization is logically grouped to minimize the number of lines required for VLSI interface ICs. The net result is a bus structure that's entirely different from ISA.

Compatibility: EISA's watchword

In contrast, one of the driving forces behind the EISA connector is compatibility with existing ISA boards. After receiving several design proposals, the consortium has adopted a bilevel-connector design by the Burndy Corp. The connector has 192 pins arranged in two levels of contacts. The upper level is compatible with the ISA bus, and the lower level defines the pins for the EISA standards (**Fig 1**).

Key elements in the design are

slots in the connector body that permit notched, 32-bit plug-in cards to interconnect with the lower level of contacts. The slots block existing 8-and 16-bit, ISA-style cards from touching the lower contact level. Therefore, ISA-style cards use only the upper contact level, which is 100% compatible with the ISA bus.

The EISA connector has the same dimensions as the current 98-pin ISA connector. It adds 55 new signal pins and a number of distributed-power and -ground pins. In addition, EISA add-in cards have 63 in² of usable board space and can use 4.5A from the 5V power supply. In contrast, an MCA card has only 36 in² available for building circuitry, and it's limited to a maximum of 2A from the 5V supply.

Noise is a nasty interrupt

Both architectures offer many similar capabilities, but the ISA-compatibility issue influences their implementation. For example, the ISA bus has active-high interrupt lines so that only one board can use a specific interrupt line, thus limiting the number of interrupt-driven devices. In addition, the interrupts are edge triggered, making them susceptible to noise spikes.

The MCA permits multiple devices to share a common interrupt line. The MCA has eight available, active-low, interrupt-request lines. You can connect more than one interrupt source to the same interrupt-request line in a wired-OR fashion, using open-collector drivers. Each device that wishes to share an interrupt-request line must set a bit in an I/O register to indicate that it requires service. The interrupt-service routine polls the bit for a particular interrupt level to see which adapter generated the interrupt. After servicing the interrupt, the routine resets the bit.

The EISA specification supports

EISA vs MCA

both edge-triggered, active-high interrupts and shared, active-low interrupts. It uses the same 11 interrupt lines defined on the ISA bus. Existing ISA cards can use the edge-triggered protocol, but they must use a dedicated interrupt line. New EISA cards can share an interrupt line, but they must have an I/O register that indicates which board set the interrupt, similar to the MCA. The system board contains an edge/level triggered register that the operating system can interrogate for the status of each interrupt configuration.

Both architectures define different types of bus cycles for data transfer. The MCA is defined as an asynchronous bus because it doesn't have a common bus-clock line. Its synchronous-default bus cycle is synchronized to the current bus master's CPU clock, and it's specified as 200 nsec min. The cycle begins when the master asserts the ADL (address decode latch) signal. indicating that the current bus address is valid. The ADL signal lasts for 1 CPU-clock period. The master then asserts the $\overline{\text{CMD}}$ (command) line to transfer the data. The CMD line lasts for 3 CPU-clock periods in no-wait-state designs. Therefore, a synchronous-default bus cycle requires 4 CPU-clock cycles. A system that has a 16-MHz CPU (a 62.5-nsec CPU-clock period) has a no-wait-state, synchronous-default cycle of 250 nsec.

A slave that can't operate at the default speed has two options for extending the bus cycle: it can transfer the data via a synchronous or asynchronous extended cycle. First, the slave must negate the card channel-ready line in response to the master's assertion of the (\overline{ADL}) signal. The way the slave reasserts the channel-ready line determines whether the data transfer occurs via a synchronous or asynchronous extended cycle. If the slave reasserts the channel-ready

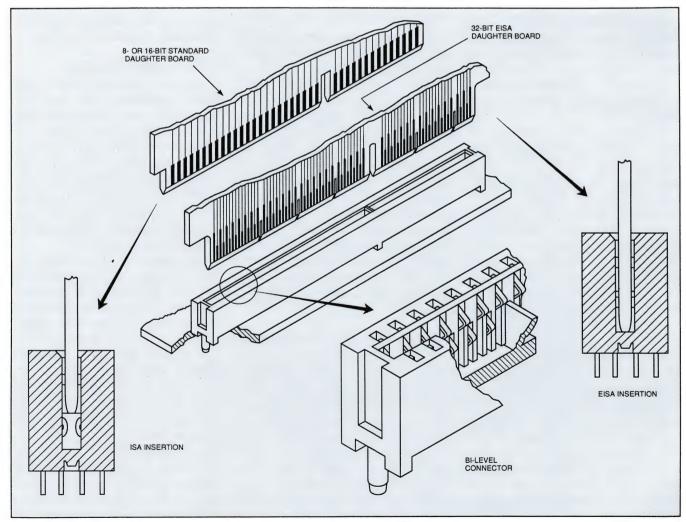


Fig 1—The EISA bus connector features a bilevel arrangement of contacts. The Burndy connector has slots that allow EISA cards to be fully inserted, but ISA cards can connect only to the upper level of contacts.

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EISA vs MCA

line in response to the assertion of the \overline{CMD} line by the master, the bus cycle is synchronously extended by 1 CPU-clock period. The asynchronous extended cycle lengthens the bus cycle until the slave asynchronously reasserts the channel-ready line within 3 μ sec.

In addition, IBM PS/2 machines (such as the Model 80) that support 32-bit data transfers have a matched-memory bus cycle that requires only 3 CPU-clock periods (187.5 nsec for 16-MHz machines). A 32-bit-wide memory card can request the use of this bus cycle by asserting a matched-memory-cycle request (MMCR) signal when the current bus master addresses the memory card.

The DMA controller in the current models of the PS/2 computer, however, don't support 32-bit DMA transfers. The controller transfers 8- or 16-bit data using a single transfer or a burst mode. In burst mode it transfers data a minimum of every 500 nsec on the MCA bus. Therefore, the maximum DMA burst-transfer rate is 4M bytes/sec when transferring 16-bit words.

EISA uses a synchronous bus clock

The EISA synchronous bus has an 8.33-MHz bus-clock line, and the EISA specification defines a variety of synchronous bus cycles. The only available VLSI devices that implement the standard are in Intel's 82350 EISA bus chip set. The set includes two system-board devices: the 82358 EISA bus controller (EBC), which costs \$120 (1000); and the 82357 integrated-system peripheral (ISP), which costs \$99 (1000). The set also features an addin-board interface chip, the 82355 bus-master interface controller (BMIC), for \$35 (1000). The ISP incorporates a DMA controller, an interrupt controller, bus arbitration, and dynamic RAM (DRAM) refresh functions.

	MINIMUM	1
DMA TIMING MODE	CYCLE-TRANSFER TIME (nSEC/ SINGLE CYCLE)	MAXIMUM DATA-TRANSFER RATE (M BYTES/SEC)
COMPATIBLE	1000	4.17
TYPE A	750	5.56
TYPE B	500	8.33
TYPE C (BURST MODE)	120 (1 BUS-CLOCK PERIOD)	33.33

The EBC facilitates the execution of bus cycles between the host CPU and the EISA bus. Because EISA includes all of the ISA features, the EISA bus cycles can be considered a superset of the ISA bus cycles. The current bus master must synchronize the start of the bus cycle to the bus clock. After synchronization, the master issues a \$\overline{START}\$ command that lasts for 1 bus-clock period. The \$\overline{START}\$ signal is functionally equivalent to MCA's \$\overline{ADL}\$ signal.

The bus master then asserts the $\overline{\text{CMD}}$ line, which lasts for another bus-clock period. The rising edge of the bus-clock signal transfers the data while the $(\overline{\text{CMD}})$ signal is low. The standard bus cycle with no-wait states lasts for 2 bus-clock periods. An EISA slave can also request a compressed bus cycle that lasts for 1.5 bus-clock periods.

EISA's 8.33-MHz bus-clock frequency defines a minimum bus-clock period of 120 nsec. Slave devices insert wait states using the channel-ready command or an EISA Ready signal that's synchronous with the bus-clock period. The specification is similar to that of the MCA, in that it defines a combination of 8-, 16-, and 32-bit data transfers. Intel's EBC performs the translation algorithm necessary to assemble the bus cycles according to the master and slave size.

In addition, the ISP's DMA controller transfers data using four DMA timing modes (**Table 1**). Slow DMA slaves can use the compatible timing mode, which transfers data at 1000 nsec/cycle. Fast 32-bit DMA slaves can use a burst mode, which transfers a 32-bit word on every bus clock. DMA slaves designed to use the burst mode can achieve a 33.33M-byte/sec transfer rate.

A major difference between the two architectures lies in the most touted feature of both—bus arbitration for multiple bus masters and DMA slaves. MCA uses a distributed-arbitration protocol, and EISA uses a centralized protocol.

The MCA bus features a central-arbitration control point located on the system board. The control point supports as many as 16 arbitrating devices, such as a DMA slave, a bus master, or the system CPU. Arbiters initiate an arbitration cycle by driving the PREEMPT line active. The control point indicates that an arbitration cycle is in progress by driving the ARB/GNT line to the arbitrate state.

The arbiters then drive their assigned 4-bit arbitration levels (ARB0 through ARB3) onto the arbitration bus. Any arbiter that sees an arbitration value on the bus that's lower than the value assigned to it must stop driving the bus. Therefore, the lowest arbitration level wins control of the bus when the control point places the ARB/ GNT line into the grant state.

To implement the MCA arbitra-

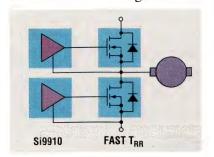
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EISA vs MCA

tion scheme, each potential arbiter on the bus must contain circuitry that performs the back-off algorithm. Fortunately, vendors of interface chips for the MCA include this circuitry in a number of their ICs. Capital Equipment's 88C01, Chips and Technology's 82C612, Data Translation's DT7920, and PLX Technologies' MCA 1200/1210 are several interface ICs that support the arbitration logic (Ref 1). The ICs also support a fairness algorithm that prohibits a high-priority arbiter from "hogging" the bus.

Intel's 82357 ISP implements EISA's centralized arbitration protocol on the system board. The arbitration unit assigns each of the bus arbiters to a slot at a specific interrupt level in a rotating priority scheme. For example, the interrupt level for the eight DMA channels

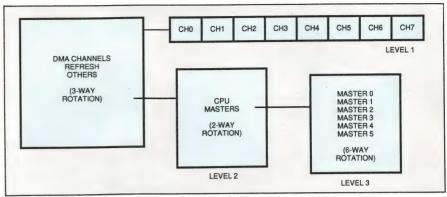
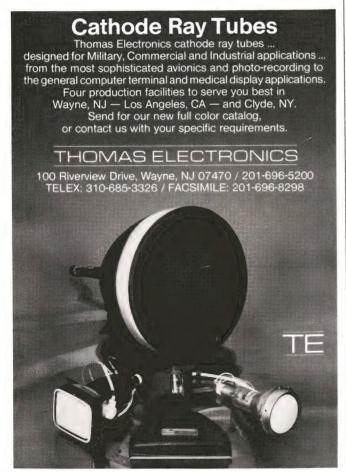


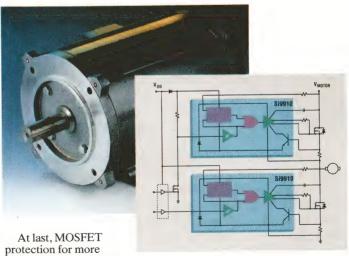
Fig 2—EISA's centralized arbitration unit determines an arbiter's priority on a rotational basis. The unit assigns equal weights to each arbiter at each level.

considers all the DMA channels equal and are given an 8-way rotation. Similarly, the interrupt level for the six bus masters considers them equal and are given a 6-way rotation. The system CPU is the default master when no other requesters exist. An example of the

priority assignments is shown in Fig 2. Essentially, the rotating priority assignments provide a fairness protocol that prevents high-priority devices from "hogging" the bus. For example, a system that has a CPU, two bus masters (M1 and M2), and a DMA slave that's using



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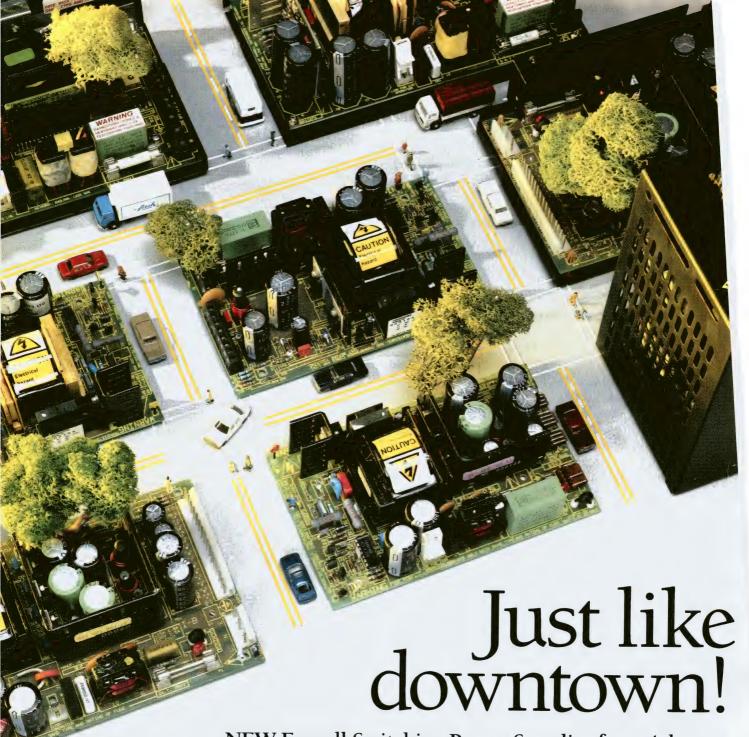


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EISA vs MCA

the second DMA channel (DMA2) rotates in the following sequence:

 $\rightarrow DMA2 \rightarrow CPU \rightarrow DMA2 \rightarrow M1$ $\rightarrow DMA2 \rightarrow CPU \rightarrow DMA2 \rightarrow M2 \rightarrow$

An EISA bus master arbitrates for the bus by issuing an \overline{MREQx} (memory request) signal that's assigned to an individual bus slot (x indicates the slot number). The master receives a grant when the system arbiter issues a \overline{MACKx} (memory acknowledge) signal—another slot-dependent signal. EISA bus masters must release the bus within 64 bus-clock periods (8 μsec) if the system arbiter negates the \overline{MACKx} signal. A 16-bit ISA master can use an ISA DREQ (DMA request) line, and it can't be

pre-empted from the bus.

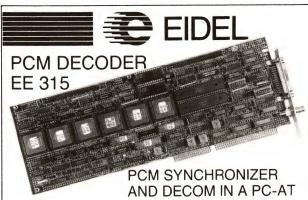
None of the current versions of interface ICs for the MCA offers a complete set of bus-master functions in one circuit; a bus master must issue all the address, data, and control signals in the bus cycle. PLX Technology's 1200 and 1210 chips can issue the command (CMD) line for the MCA bus cycle, but they require a number of external latches and logic circuitry to handle address, data, and control lines for the 80386 pipelined architecture. Generally, you must perform the additional logic in a PLD.

In contrast, Intel's BMIC contains several elements that allow it to perform single and burst transfers for a bus master. This device includes the arbitration logic to gain ownership of the bus; two address counters to handle the EISA ad-

dresses during data transfer; two FIFO buffers to insulate the local bus from the EISA bus; data shifters to align the FIFO buffers on arbitrary byte boundaries; command and status registers for passing EISA commands; and an EISA slave interface for communication with the system CPU.

In response to customer requests, Intel also built a number of "bells and whistles" into the BMIC. Peek and Poke registers allow a local μ P to communicate with I/O and memory devices over the EISA bus. The BMIC also has a set of identification registers; a pair of semaphore ports; two 8-bit doorbell registers for interrupts; and a set of four 32-bit mailbox registers.

The EISA specification also defines automatic configuration on power-up, using registers similar to



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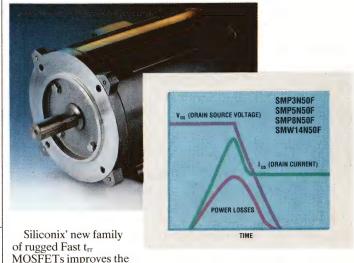
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CIRCLE NO 8

TECHNOLOGY UPDATE

For more information . . .

For more information on the EISA and MCA products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Burndy Corp Box 5200 Norwalk, CT 06856 (203) 838-4444 Circle No 716

Capital Equipment Corp 99 S Bedford St, #107 Burlington, MA 01803 (617) 273-1818 Circle No 717

Chips and Technologies Inc 3050 Zanker Rd San Jose, CA 95134 (408) 434-0600 TLX 272929 Circle No 718 Data Translation Inc 100 Locke Dr Marlboro, MA 01752 (508) 481-3700 FAX 508-481-8620 Circle No 719

Intel Corp Box 58065 Santa Clara, CA 95051 (800) 548-4725 Circle No 720 Micro Computer Systems Inc 5005 Royal Ln, Suite 104 Irving, TX 75063 (214) 929-4182 FAX 214-929-0838 Circle No 721

PLX Technology Inc 625 Clyde Ave Mountain View, CA 94043 (415) 960-0448 Circle No 722

the MCA programmable-optionselect (POS) registers. The EISA consortium and Micro Computer Systems (MCS) have developed an EISA-configuration utility program that permits software to read a board's identification and configure its setup registers. The system BIOS reads the utility and configures the system during power-up.

The utility also displays the DIPswitch configuration on a monitor in the system to avoid configuration conflicts with older ISA boards. MCS will license the utility to hardware and board manufacturers. Vendors can provide the utility on system setup disks.

IBM's configuration utility comes with a PS/2 computer. The PS/2 enjoys a 2-year head start over EISA computers in many areas of customer acceptance. Also, MCA currently has a large and growing hardware and software base.

Many uncertainties in EISA's development remain. For example, interface-chip vendors are reluctant to develop EISA chips because of the numerous specification changes that have occurred since EISA's inception. The first EISA computers will use the Intel chip set, so other IC vendors are concerned that any

specification ambiguities could cause their chips to malfunction. In addition, IC vendors are concerned about how the consortium will handle licensing agreements and the distribution of the EISA specification. Currently, this so-called "open architecture" is only available to developers under a nondisclosure agreement. An independent law firm—Bishop, Cook, Purcell, & Reynolds (BCPR Services)—handles the distribution and charges each developer a \$2500 fee. This fee could discourage many developers and hamper EISA in its bout with MCA. EDN

References

- 1. Conner, Margery, "Micro Channel Interface ICs," *EDN*, June 8, 1989, pg
- 2. Embler, Gary and Michael Slater, "EISA extends AT Bus Definition," Microprocessor Report, July 1989, pg 11.

Article Interest Quotient (Circle One) High 506 Medium 507 Low 508



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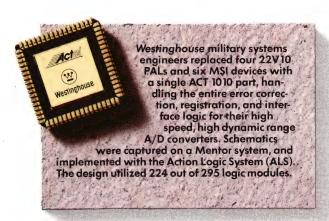
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CIRCLE NO 64

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more with Actel, you also get less.
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For engineers at Siemens Medical Electronics, using the Actel System for both production and design cut the production cycle by an estimated two months. They produced the working prototype of their new pulse oximetry device only two weeks after delivery of the Action Logic System. And all the complex glue logic around the microprocessor was implemented on one 1200-gate ACT 1010 chip.

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And it comes in a range of sizes, with 1,200- and 2,000-gate parts today, and 6,000 gates on the way.

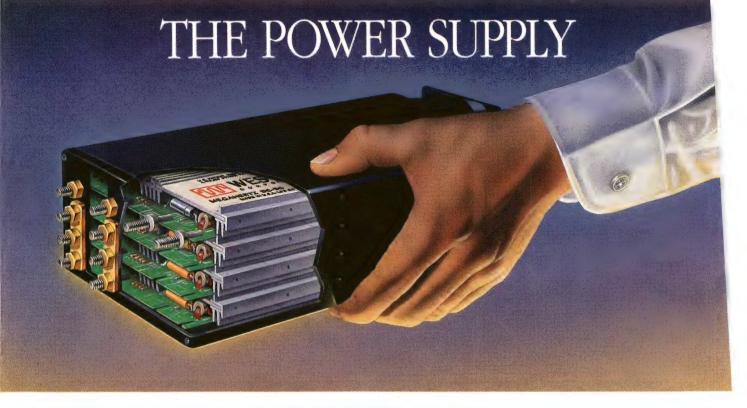
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Model	Output Voltage (VDC) and Maximum Current											
	(amperes) per Channel											
	#1	#2	#3	#4	#5							
Single Outpu	ıt											
SP1-1801	2@240											
SP1-1802	5@240	Total output power may not exceed 1200 watts for any model, single										
SP1-1803	12@100											
SP1-1804	15 @ 80											
SP1-1805	24@50	or multiple output. Lower power StakPak models are available.										
SP1-1806	28 @ 42	Please contact the factory.										
SP1-1807	48@25											
Dual Output												
SP2-1801	2@120	5 @ 120										
SP2-1802	5@120	5 @ 120										
SP2-1803	5 @ 120	12@66										
SP2-1804	12@66	12@66										
SP2-1805	15 @ 53	15 @ 53										
Triple Outpu	ıf											
SP3-1801	5 @ 180	12@16	12@16									
SP3-1802	5 @ 150	12@33	12 @ 16									
SP3-1803	5 @ 180	15 @ 13	15 @ 13									
SP3-1804	5 @ 150	15 @ 26	15 @ 13									
Quad Outpu	ıt											
SP4-1801	5 @ 150	12@16	12 @ 16	5@30								
SP4-1802	5 @ 150	15 @ 13	15 @ 13	5 @ 30								
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24 @ 8								
SP4-1804	5 @ 150	15 @ 13	15 @ 13	24@8								
Five Output												
SP5-1801	5@120	12@16	12 @ 16	5 @ 30	24@8							
SP5-1802	5 @ 120	15 @ 13	15 @ 13	5 @ 30	24@8							



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PROGRAMMABLE LOGIC

PLD architectures require scrutiny



Selecting an efficient field-programmable gate array or high-gate-count PLD often means matching the correct device architecture to your application. Therefore, you must know the strengths and weaknesses of each device.

Doug Conner, Regional Editor hen you look at highgate-count programmable devices, whether PLDs or field-programmable gate arrays, you'll see a variety of different architectures. Trying to find the proper architecture for your application can be confusing.

One way to cut through some of the confusion is to look at these devices from the perspective of how many flip-flops you can use. Or, if the device has too many flip-flops, how many you will waste. The number of flip-flops is easy to determine both in your design as well as in the programmable device itself. Furthermore, you usually can't get the job done if you have too few flip-flops. Of course, the number of flip-flops you need depends on which type of flip-flop the device has.

You'll see by looking at **Table 1** that considerable differences exist in the number of flip-flops available. The **table** lists the highest gate-count devices that are currently available (or will be in the near future) from the listed vendors. Many vendors also have a number of devices with fewer equivalent gates, and with correspondingly fewer flip-flops. You must consider many factors when examining the number of flip-flops on these devices. You need to know how they fit into the overall architecture of the devices before determining their usefulness for your application.

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With its 9000 equivalent gates, the Xilinx XC3090 currently dwarfs all other devices. Not surprisingly, it has the highest number of possible flip-



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CIRCLE NO 67

silicon systems°

Programmable logic

flops. Note also that this device has the highest number of dedicated flip-flops—that is, gates configured only as flip-flops. If your design calls for few flip-flops, you could easily be wasting 2000 or 3000 equivalent gates. However, if your designs are register intensive, you'll have plenty of equivalent

gates available.

The logic-cell-array architecture of the XC3090 comprises a perimeter of 144 programmable I/O blocks (each block contains 2 flip-flops), 320 configurable logic blocks, plus an interconnect structure. Fig 1 shows a configurable logic block's basic structure. The combinatorial

function block uses a 32×1-bit lookup table to perform any 5-variable Boolean logic function, any two 4variable functions, and even some 6- and 7-variable functions. The balance of a configurable logic block includes two flip-flops and a program-memory-controlled multiplexer section, which routes sig-

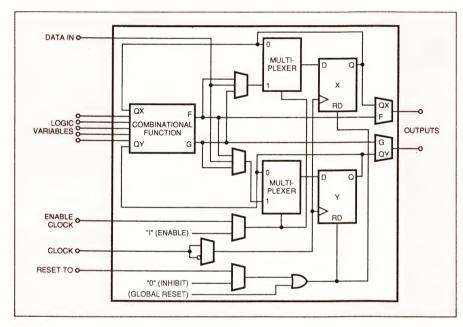


Fig 1—Three hundred twenty of these configurable logic blocks, plus 144 programmable I/O blocks, make up the Xilinx XC3090 LCA. A programmable interconnect structure ties the blocks together. The 64,160 data bits loaded into on-chip static RAM define the configuration.

TABLE 1—REPRESENTATIVE HIGH-GATE-COUNT PROGRAMMABLE LOGIC DEVICES

MANUFAC- TURER	DEVICE	DEVICE TYPE	PROGRAM- MING METHOD	NUMBER OF LOGIC BLOCKS ON MACRO- CELLS	DEDI- CATED FLIP- FLOPS	MAXIMUM POSSIBLE FLIP- FLOPS	MAXI- MUM FLIP- FLOP TOGGLE RATE (MHz)	SINGLE- LEVEL PROPA- GATION DELAY INPUT TO OUTPUT (ASEC)	STANDBY POWER (mA)	OPER- ATING POWER (MHz)	INPUT ONLY PINS	OUTPUT ONLY PINS	I/O PINS	PRICE	ALTERNATE SOURCE
ACTEL	ACT1020	CMOS	ANTIPOSE	546	0	273	70	21	10	26	0	0	69	\$79.19 (100s)	TEXAS INSTR.
ALTERA	EMP5128	CMOS	EPLD	128	128	170	50	30	150	155	8	0	52	\$96.00 (100s)*	CYPRESS
ICT	PA7040	CMOS	ELEC- TRICALLY ERASABLE	24	60		50	23	120	121	14	0	- 24	\$27.80 (100) AVAILABLE FIRST QUARTER 1990	GOULD AMI
INTEL	5AC324	CHMOS	EPLD	24	34	34	50	30	0.15	20	12	0	24	\$21.50 (10,000)	
SIGNETICS	PLHS502	BIPOLAR	FUSE	8+8+64	16	32	50	22+8	250	250	24	16	8	\$14.00 (1000)	
XILINX	XC3090	CMOS	STATIC RAM	320	928	928	100	20	2.5	26	0	0	144	\$311.00 NOW (1000) \$102.00 SECOND QUARTER 1990	

NOTE: *=CERAMIC PACKAGE WITH WINDOW

Programmable logic

nals within the configurable logic block.

If you contrast the logic-cellarray architecture with Actel's ACT1020, you'll note a considerable difference. Fig 2 shows the logicmodule building block for the ACT1020. The 8-input, 1-output logic module can implement a variety of functions, including all 2-variable Boolean functions, and some 3-and 4-variable Boolean func-

tions. The module can also implement a 4:1 multiplexer. You can construct latches from one module; flip-flops require two.

Because you build every function from these logic modules (546 of them on the ACT1020), you never waste a large number of logic blocks on functions you may not need, such as too many flip-flops. Such flexibility lets Actel claim 85 to 95% of the useable gates on almost any design.

One aspect you need to keep in mind when thinking about the ACT1020's architecture is the trade-off of logic modules between flip-flops and other logic functions. If you design a circuit using all 273 flip-flops available on the ACT1020, you'll have no logic modules left for combinatorial functions.

The device architectures of both the Xilinx logic-cell array and the

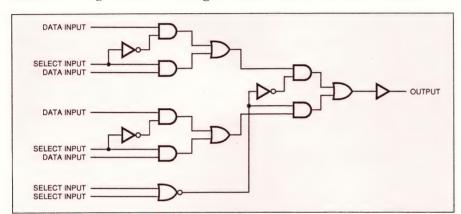


Fig 2—The 8-input, 1-output logic module is the basic building block for Actel's ACT1 family of parts. A variety of logic functions, including latches and a 4:1 multiplexer capability, can be constructed from each of the 546 modules available on an ACT1020. An extensive library of macros relieves you of ever having to design with the logic module itself.

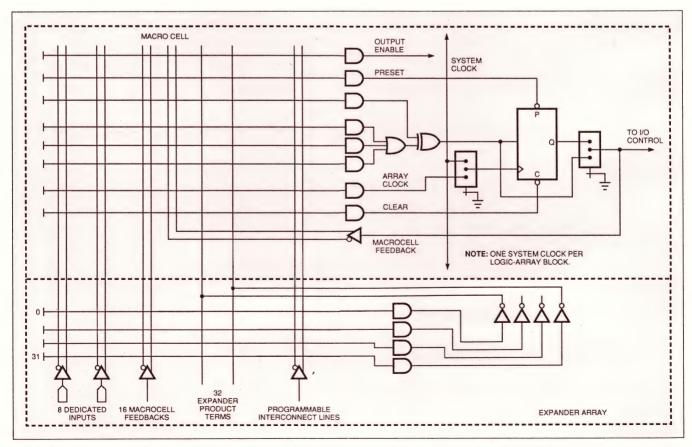
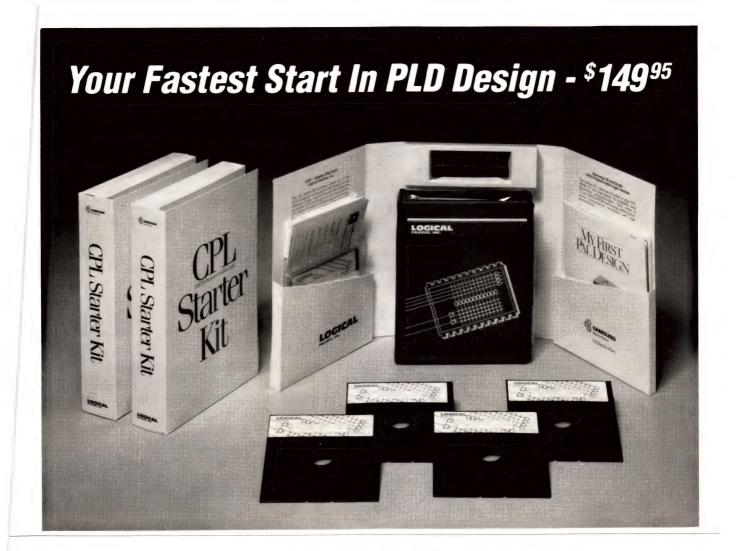


Fig 3—Each of the eight logic-array blocks in Altera's EPM5128 contains 16 macrocells plus a 32-product-term expander array, which lets you use more than three product terms for those macrocells where you require them.



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Programmable logic

Actel ACT1 family are quite different from the programmable-AND, fixed-OR architectures common in PLDs. Altera's multiple-array-matrix family uses a variation of the basic PLD architecture. Rather than just trying to make a huge PLD, which often wastes many gates, it took a hierarchical approach, grouping 16 macrocells in each of eight logic-array blocks on its EPM5128.

Altera has done something more significant than just grouping eight PLDs with an interconnect structure on a chip. The three product terms feeding the OR gate in Fig 3 will handle the majority of designs and never waste more than two product terms per macrocell. Three product terms, however, won't handle *all* designs. If Altera's designers had added more product-term inputs to each macrocell, the gates

would simply be wasted in the majority of designs.

Instead, Altera added what it calls an "expander array" of uncommitted NAND gates that you can use in cases where you need more product terms. The uncommitted NAND gates are also available as "glue logic" or any other logic function you need, including additional registers.

Signetics took another approach to getting lots of logic on a programmable device. It uses what it calls programmable macrologic in its PLHS502 Fig 4. The device has much in common with the expander array in Altera's multiple-arraymatrix architecture. The chip's large NAND-gate array feeds back on itself, and 16 of the NAND gates drive flip-flops. After your signals have run around the NAND gates' feedback loop enough times to per-

form the desired logic functions, a group of AND gates collects the outputs.

The PLHS502 will not waste product terms because each logic gate is used individually. The large number of inputs to each NAND gate results in high gate utilization in designs where each product term requires many inputs, such as in an address-decode application.

With only 16 dedicated registers and the ability to construct about 16 more with the uncommitted NAND gates, the chip does not suit register-intensive applications. Although gate-utilization percentages will be somewhat application dependent, the device can perform any Boolean-logic function and do so with low propagation delays—8 nsec for each loop through the NAND array. The full matrix of interconnects prevents you from run-

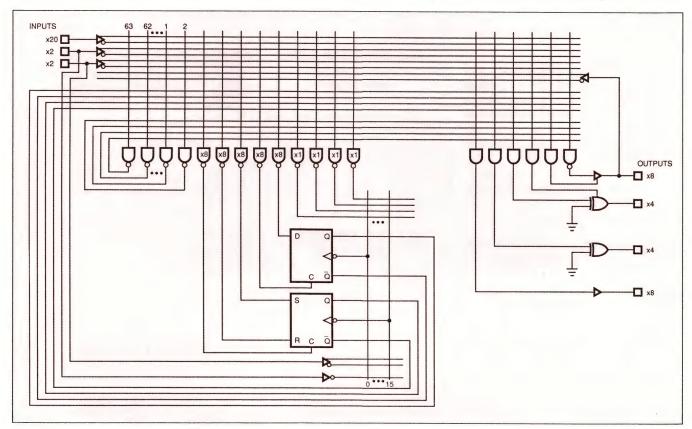
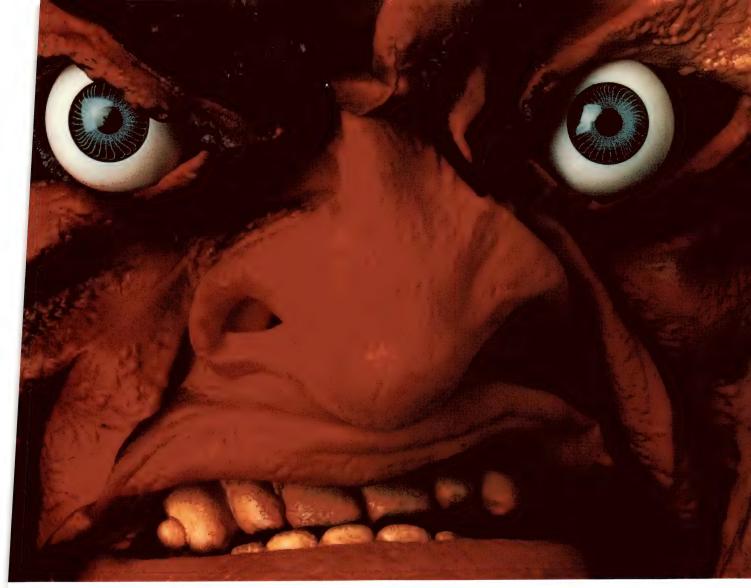


Fig 4—A large NAND-gate structure that feeds back on itself is the conceptually simple, yet flexible, structure of the PLHS502 from Signetics.



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EDN September 28, 1989 CIRCLE NO 69

Programmable logic

ning out of routing resources, a guarantee that other device manufacturers can't make.

No waiting for product terms

Intel, with its 5AC324, took yet another approach to getting high utilization of product terms. Fig 5 shows the macrocell building block for this device. Although the device nominally has eight product terms summed for each of the 24 macrocells (not including clock and control product terms), the product terms are switchable in banks of four so that a macrocell can use anywhere from 0 to 16 product terms by robbing banks of four product terms from its neighboring macrocells. When you need 16 terms you get them with no added delay. This feature contrasts with Altera's multiple-array-matrix architecture,

which adds a delay in going through the expander array for sums requiring more than three product terms. Delay times for these devices are listed in the **table**.

To get high gate utilization when designing with the 5AC324, your design should use product terms that require wide inputs. Also, you need to average close to eight product terms per macrocell over the entire device or you'll be wasting product terms. You're limited to one flip-flop per macrocell, plus 10 registered input cells.

One way to get the optimal number of products for each sum in a sum-of-products architecture is to have both a programmable-AND array and a programmable-OR array. The PA7040 PEEL (programmable electrically erasable logic) array from International CMOS Tech-

nology has this programmable-logic-array architecture.

You select the product terms from the programmable-AND array as needed for the four sum terms available at each logic-control cell. These cells, which aren't elements of a traditional programmable-logic architecture, each contain a register and multiplexers, and they control the signal flow within the cell. The PA7040 has a total of 120 product terms available for the 24 logic-control cells—an average of five product terms per logic-control cell.

This count is probably a generous number with this architecture because you need to generate a specific product term only once, and then you can use it as an input to several logic-control cells. Furthermore, you need never waste product terms until you reach the I/O

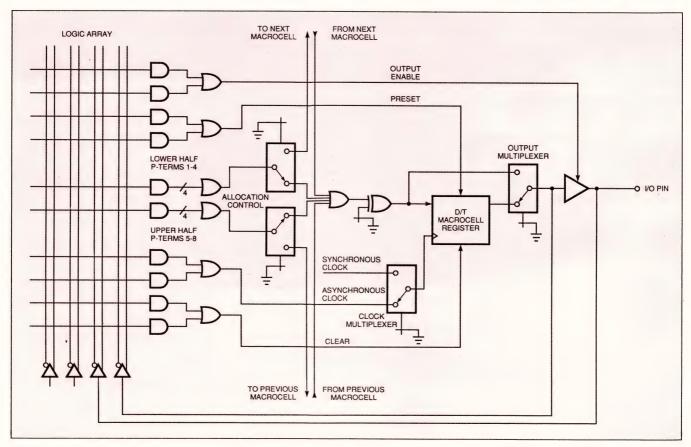
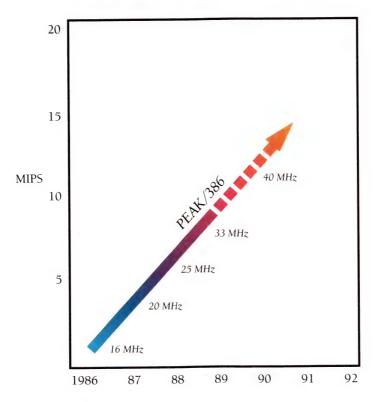


Fig 5—The ability to switch product terms in banks of four between macrocells means you can use as many as 16 product terms for one macrocell and still incur only a single-level propagation delay. Twenty four of these macrocells go into a 5AC324 from Intel.

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Programmable logic

limit of the device. The PA7040 has a flip-flop in each of its 24 logiccontrol cells plus 36 registers available in input and I/O cells.

Many applications for programmable logic must be fast. Unfortunately, specific operating-speed numbers are difficult to determine with most devices due to their flexibility. Flip-flop toggle rates, for example, are difficult to work with because even if you derate them about 60% for a typical application, that value might have to be revised down drastically if signals are fed back and have to propagate through multiple logic levels.

Even single-level propagation delays lose meaning because a single level (one logic module) on Actel's ACT1020 is hardly comparable in function to a single level in an XC3090 or a 5AC324. Interconnect delays on the XC3090 can vary widely, depending on the routing. For these reasons, you should use the speed-related values in the table only as rough indicators.

Operating power is another specification that you can determine only with difficulty for programmable devices. The power consumption of most devices will depend on the design programmed into the device and the rate at which logic elements switch states, both internally and at the outputs. Some manufacturers specify parts with only some type of counter circuit programmed into the part. Other manufacturers give detailed methods of how to compute power consumption in your application.

The operating power consumption listed in the table assumes no loads on the outputs. Loading, both resistive and capacitive, can have a significant impact on operating power consumption.

Up to this point we've been looking at products you can get your hands on right now (or by the first quarter of 1990 for the PA7040). To see how programmable-device densities will be going up, it's worthwhile to look at a few of the products that will be available within a vear.

Xilinx will introduce its 4000 Series logic-cell array with as many as 20,000 equivalent gates, and as many as 24k bits of on-chip RAM, which will be a separate RAM array available for general-purpose data storage. Actel will soon add a 6000gate product to its line.

Plessey will introduce its ERA 60100 electrically reconfigurable array. This RAM-based design contains 10,000 cells. Each cell can be a 2-input NAND gate or a D latch. The company credits the array as having 40,000 equivalent gates (it considers each cell to equal four gates for the D latch). The device with development systems is scheduled to be out in the first quarter of 1990.

Reference

1. Small, Charles, User-programmable gate arrays, EDN, April 27, 1989. pg 146.

Article Interest Quotient (Circle One) High 512 Medium 513 Low 514

For more information . . .

For more information on the programmable logic devices discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Intel Co 3065 Bowers Ave Santa Clara, CA 95051 (408) 765-8080 Circle No 711

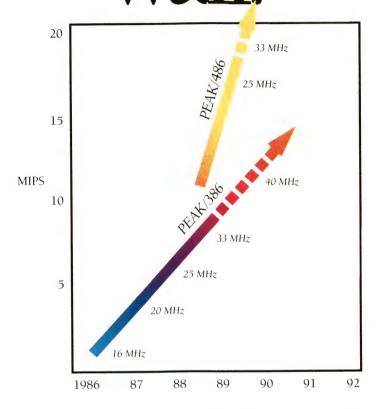
Plessey Semiconductors 1500 Green Hills Rd Scotts Valley, CA 950 (408) 438-2900 FAX 408-438-5576 Circle No 712

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RISC µP features 66-MIPS performance and includes interrupt and DMA controllers

Targeting embedded-processor applications, the i960CA RISC (reduced instruction set computing) μP regularly executes two instructions per clock cycle. The μP , offered at speeds as fast as 33 MHz, achieves a native-instruction peakperformance level of 66-MIPS. The processor offers code compatibility with the 80960KA μP introduced last year. The i960CA μP , however, includes DMA, bus, and interrupt controllers that allow you to use the processor in embedded designs with a minimum of support chips. Fur-

thermore, you can choose from a number of key memory and peripheral ICs designed specifically for the new μP .

Key architectural features of the i960CA that allow the processor to execute multiple instructions per clock cycle include parallel instruction decoding; a 1k-byte, 2-way set-associative instruction cache; multiple parallel-execution units; a multiport register file with scoreboarding; multiple internal buses; and an on-chip interface to peripheral ICs via the DMA, bus, and inter-

rupt controllers (see Fig 1).

The instruction sequencer fetches instructions from the cache, the Macro ROM, and the instruction queue that holds prefetched instructions. A pipe sequencer can examine four instructions per clock cycle. The sequencer directs the instruction stream into individual control, register, and memory parallel pipelines. Memory and register instructions execute and return a result in a single clock cycle.

The Multiply/Divide, Integer Execution, and Address Generation

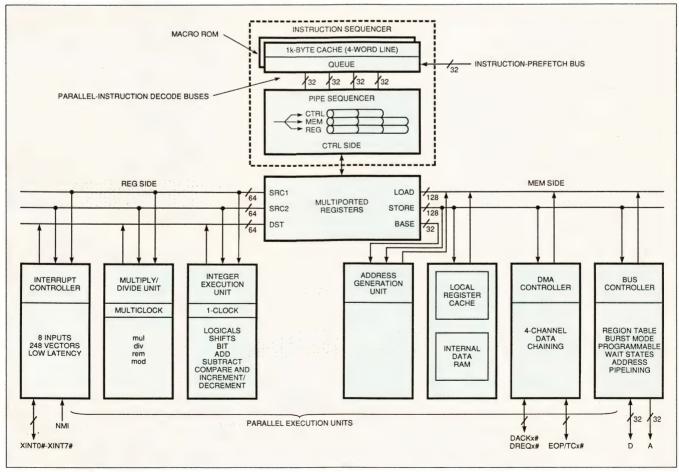


Fig 1—A pipeline instruction sequencer, a large register file with a scoreboard, multiple execution units, and a local register cache allow the i960CA to regularly execute two instructions per clock cycle.

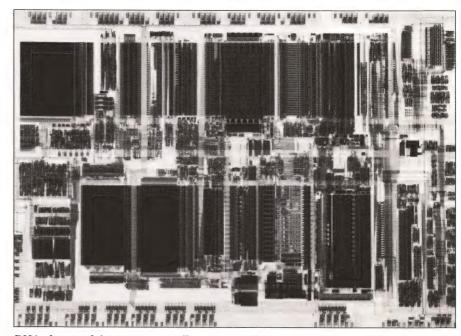
PRODUCT UPDATE

Units make up the core of the µP architecture. The register scoreboarding feature manages the instructions that are issued to the execution units. The register file includes 16 local registers, 16 global registers, and 32 literals for immediate data operations. Each register is 32 bits long plus 1 scoreboard bit. The file includes four independent read ports, two independent write ports, and a control port. The architecture also includes a local register cache that stores a minimum of six register sets on chip at all times. The cache speeds context switching.

The DMA, bus, and interrupt controllers reduce the chip count-in designs and supply the μP with the high-speed data stream needed for efficient operation. The bus controller can read data at a 132M-byte/sec rate and write data at a 106M-byte/sec rate. The controller queues both loads and stores and includes a memory-region configuration table that can size the bus to 8, 16, or 32 bits and set wait-state parameters by region. The controller also supports address pipelining for burst-mode operation.

The 4-channel DMA controller supports data transfers as fast as 59M bytes/sec and can transfer data at 32M bytes/sec with no effect on user-program execution. DMA instructions perform a complete channel setup in 12 clock cycles. The DMA controller also supports data chaining for linked-list and scatter/gather operations.

The multimode interrupt controller has an expanded mode that can support 248 external interrupt sources. The dedicated mode supports eight interrupts directly sourced by interrupt pins. A mixed mode allocates three external pins for dedicated interrupts and five



DMA, bus, and interrupt controllers integrated on the i960CA μP make the 33-MHz, 66-MIPS RISC processor ideal for embedded applications that require a small chip count.

pins to set a vector for expandedmode operations. The controller accepts four DMA-sourced interrupts and a nonmaskable interrupt.

Several peripheral ICs designed specifically for use with the i960CA support the chip features. For example, the 27960 burst-mode EPROM integrates directly with no glue logic to the i960CA and its bus controller. The 128k-byte (1M-bit) CMOS EPROM can support synchronous 4-byte burst transfers at speeds of 33 MHz. The EPROM ranges in price from \$21 to \$37 (10,000) for speeds ranging from 16 to 33 MHz.

The company also offers burst-mode function-specific PLDs for use with the μP . The 85C960 PLD provides address-decoding, wait-state, and ready-generation functions for the processor. The IC can generate 0 to 15 wait states across eight address ranges. A 25-MHz version of the PLD costs \$29.95 (10,000). The company also plans to offer a higher

speed PLD and a LAN coprocessor for the μP .

A number of development tools for use with the i960CA are also available. The tools include the iC960 optimizing C compiler and ASM960 macro assembler that sell for \$700 and \$900, respectively, for MS-DOS-based PCs. In addition, the company offers the \$750 SIM960CA performance simulator for MS-DOS applications, and an evaluation board should be available at the end of this quarter.

The i960CA μP is housed in a 168-pin ceramic pin-grid-array package in 16-, 25-, and 33-MHz versions that sell for \$273, \$303, and \$379 (1000), respectively. Production quantities of the i960CA will be available in the fourth quarter.

-Maury Wright

Intel Corp, Literature Dept LG42, Box 58065, Santa Clara, CA 95051. Phone in US and Canada, (800) 548-4725.

Circle No 730



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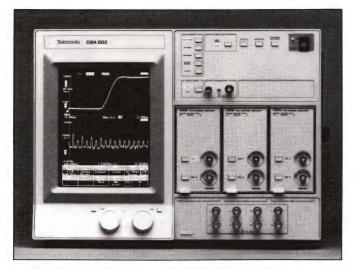
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READERS' CHOICE

Of all the new products covered in EDN's June 8, 1989, issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, use EDN's Express Request service, or refer to the indicated pages in our June 8, 1989, issue.



■ SIGNAL ANALYZERS

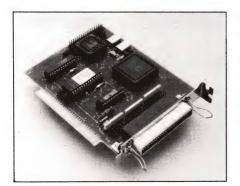
The DSA 601 and 602 digitizing signal analyzers combine real-time DSP capability with a 1-GHz-bandwidth, 2G-sample/sec digital storage oscilloscope (pg 115).

Tektronix Inc. Circle No 740

SCOPE SOFTWARE

Release 3.0 of the Snapshot Storage Scope software package requires no programming and allows acquisition, storage, and display of analog data. It supports more than 100 boards from six vendors (pg 258).

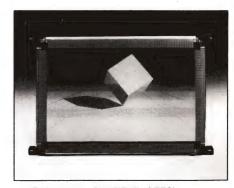
HEM Data Corp. Circle No 741



◄ CONTROLLER

The RT1000 SCSI host adapter on a half-card for IBM PCs comes with a BIOS ROM that lets you connect or boot the system to a SCSI hard-disk drive (pg 220).

Rancho Technology Inc. Circle No 742



▲ PANEL DISPLAYS

Electroluminescent displays feature 16 levels of gray scale and are available in high-temperature versions (pg 236).

Sharp Electronics Corp. Circle No 743



▲ MATH SYSTEM

The Mathematica interactive computational system for scientists and engineers runs on 80386-based computers with numeric coprocessors (pg 252).

Wolfram Research Inc. Circle No 744

SWITCHMODE ICS

The Si9115 and Si9116 CMOS ICs can operate from a rectified, filtered ac power line; handle input voltages to 300V; and provide power conversion to 250W. The devices include start-up circuitry, an oscillator, an error amplifier, and a voltage reference (pg 228). Siliconix Inc.

Circle No 745



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CIRCLE NO 74

EDN SPECIAL REPORT

8- and 16-bit MICRO-CONTROLLERS

Microcontroller prices are plunging. At the same time, manufacturers are increasing the variety of peripherals integrated on chip. The severe competition in the microcontroller market means that system designers can obtain a greater assortment of sophisticated, application-specific devices at cutthroat prices.

J D Mosley, Regional Editor

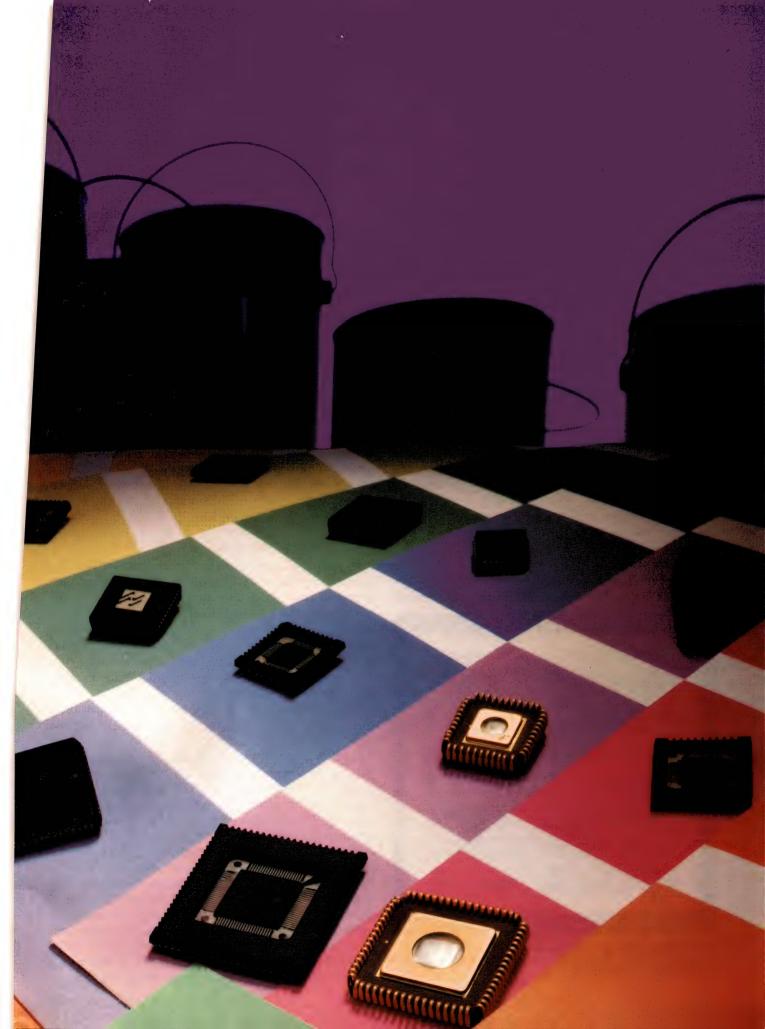
s microcontroller manufacturers battle it out for market share, the assortment of 8- and 16bit devices continues to grow, and prices continue to fall. The microcontroller market is extremely price-sensitive—a price difference as small as 10 cents can cause developers to select one microcontroller instead of another. As a result, these highly sophisticated and increasingly complex devices are often sold in high volumes as inexpensive commodities. For example, consider the price difference between microcontrollers and µPs. Although uPs represent only 6% of the total unit volume of microcontrollers and µPs sold, each of the latest µPs can cost hundreds of dollars. In contrast, microcontroller prices have dipped to less than 50 cents in volume quantities.

The modular method of producing

microcontroller families is partly responsible for the greater variety and lower prices of today's microcontrollers. In this modular approach, each manufacturer begins with a CPU core and adds modular on-chip peripherals, such as RAM, ROM, timers, and registers. The resulting microcontroller, though developed using ASIC processes, is sold as a standard product. However, the manufacturer can rapidly customize a standard microcontroller to your upgraded specifications as your product matures and your volume needs increase. Therefore, it's important to investigate your microcontroller manufacturer's plans for future development and make sure that they complement

Today's microcontrollers are produced in a modular fashion, so you can mix and match onchip peripherals to meet your upgraded specifications. (Photo courtesy National Semiconductor)



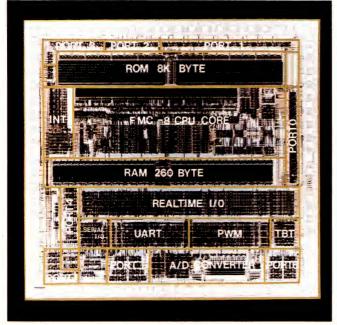


As microcontroller manufacturers battle it out for market share, the assortment of devices continues to increase, and prices continue to fall.

the path you've chosen for your product. These considerations, along with the plethora of microcontroller options, complicate the task of selecting the best microcontroller for your design.

Eight-bit devices dominate the microcontroller market. Today's microcontrollers offer improved price/ performance ratios that make it cost effective for you to upgrade your 4-bit microcontroller designs with 8-bit embedded microcontrollers. Motorola claims more than 18% of the lucrative 8-bit market, offering a selection of at least 30 standard, 8-bit microcontrollers derived from a common process. Motorola's offerings fall into two basic categories: microcontrollers built around a 68HC05 CPU core and microcontrollers built around the higher-performance 68HC11 CPU. The 68HC05 core takes about 4.5 µsec to execute an instruction, and the 68HC11 CPU executes in half that time. You can buy an MC68HC04J1 with 32 bytes of RAM, 504 bytes of ROM, an 8-bit timer, and 12 bidirectional I/O lines for as little as 49 cents (1,000,000). On the other hand, you can buy a 68HC11E9 with 512 bytes of RAM, 512 bytes of EEPROM, 12k bytes of ROM or EPROM, a 16-bit timer, and 40 I/O lines for \$10.11 (100,000).

Both cores execute software based on the ever-sofamiliar 6800 instruction set. If you already know how to program any of Motorola's 6800 family of processors,



Exhibiting the high level of integration needed to compete in the 8-bit microcontroller market, Fujitsu's MB89713 device surrounds its CPU core with RAM. ROM. and modular peripherals.

you know how to program the microcontrollers. Such prior programming knowledge helps to reduce development time, and it's part of the secret behind Motorola's market share. Motorola's adherence to the basic 6800 instruction set also ensures upward software compatibility with future microcontrollers, thus preserving the programming investment you establish in your current designs.

If you're fond of variety—and of cats—the marketers at Motorola have assembled a tablecloth-size chart of their 8-bit microcontroller assortment, each codenamed with a feline pseudonym. These chips mix and match various helpings of RAM; ROM; EPROM; EEPROM; one-time-programmable memory; A/D converters; free-running counters; watchdog timers; phase-locked loops; LCD drivers; vacuum fluorescent display drivers; and serial interfaces. Fabricated in Motorola's high-density CMOS process, these low-power devices also let you stop the clock during static periods and can shift from low- to high-speed operation to further limit power consumption.

If speed is what you need...

If you aren't attracted to the security offered by familiar instruction sets, but instead seek higher performance from your microcontrollers, the Japanese silicon giants provide an inviting selection of microcontrollers based on proprietary cores. However, these companies still follow the same modular philosophy that has permeated the industry. Each begins with a core CPU and adds modular peripherals to create a family of standard microcontrollers.

NEC, for example, proudly asserts a dedication to throughput—citing a minimum instruction cycle of 333 nsec for its μCOM-78K Series 8-bit CPU core. A fetch bus and a prefetch function further enhance throughput, as do a high-level interrupt microcontroller and its Macro Service functions. The interrupt microcontroller and its Macro Service functions reduce CPU overhead by providing data transfer in bytes or words between the chip's memory and peripherals via a specially dedicated channel. In addition, Macro Service can perform autodifferencing functions without CPU intervention. Also, to help reduce the noise that can arise from all this fast-paced activity, NEC designed this CMOS family with a parallel architecture.

You can order standard microcontrollers in this family with as much as 16k bytes of ROM and 640 bytes of RAM on chip. A memory expansion interface lets each microcontroller access as much as 1M byte of

How to select the best microcontroller for the job

The number of available microcontrollers is staggering—and manufacturers are constantly expanding the families they offer. But if you merely install the cheapest chip you can find into your circuit, you could jeopardize the viability of your product. Follow these guidelines to help you determine which microcontroller will best suit your application.

- First, consider what you really need. How much ROM?

 How much RAM? Which peripherals?
- The chip's architecture can aid your design, so compare CPU cores for performance and programming benefits. If you choose a popular CPU, more third-party tools and second sources will be available if your manufacturer stops making that device. In addition, remember that low CPU overhead is critical in maximizing performance. Further, a broad selection of peripherals wedded to a common core provides an upgrade path that will let you re-use existing code and development tools.
- Look for EPROM and EEPROM versions to ease prototyping and initial preproduction runs. Make sure that the EEPROM versions are the same size as a masked part.
- Does the chip allow external memory expansion?
- Consider the manufacturer's fabrication process.

- Are all the modular peripherals CMOS? Are some NMOS? Also, does the process offer power-saving features?
- Does the company offer a variety of packaging options? Packaging selection provides you with flexibility in manufacturing and assembly.
- Use evaluation boards and emulators to see how the microcontrollers function; don't rely solely on the specifications. Statistical data can hide architectural deficiencies such as an inefficient use of memory.
 Make sure that the prototype device you use matches the microcontroller with respect to form, fit, and function.
- How extensive are the microcontroller's software-development tools, and will they suit your needs? Is a cross assembler available to run on your IBM PC or engineering workstation? How difficult will it be to debug your code? Does the instruction set allow compact, efficient, and easy coding?
- Consider the ruggedness of the microcontroller. Does the chip contain any ESDprotection circuits? Does it have a watchdog timer or software traps? Look for a wide voltage operating range.
- Has the company provided

- the means to meet your quality and testability requirements?
- Does the microcontroller family offer a suitable upgrade path? Will this chip support derivations of your product? What are the manufacturer's plans for future generations of the family?
- Consider future designs: pin-compatible upgrades are critical. When your upgrade requires more complex functions, will you be able to add code and use the same pinout, or will you have to completely rewrite your program and redesign your circuit?
- Is the company big enough to supply your future manufacturing volumes? And at what volume can the company supply a custom derivative of the microcontroller?
- How accessible is the technical-support staff? Does the company offer a 24-hour, electronic bulletin board?
- Will the company be a microcontroller supplier in future years? Or, for that matter, is the company currently stable? After all, you need to make sure they can deliver parts today as well as in the future.
- Last—but by no means least—make sure you have the *latest* data books.

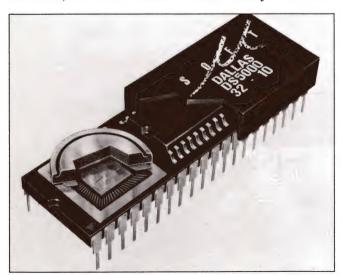
If you merely install the cheapest chip you can find in your circuit, you could jeopardize the viability of your product.

more data. The instruction set includes multiplication and division instructions, and it allows bit manipulations and BCD adjustments. You can also order onetime-programmable versions for prototyping and preproduction runs.

If the μCOM-78K sounds like overkill for your application, consider the less exotic \(\mu \colon COM-87\) family, which includes both CMOS and NMOS members. The µCOM-87 CPU core runs at a maximum frequency of 15 MHz. It uses a set of 153 instructions that include 16-bit arithmetic, multiply, and divide functions, thanks to an on-chip, 16-bit ALU. This family includes versions that contain a maximum of 16k bytes of ROM and 256 bytes of RAM on chip, and certain versions include external memory addressing for a maximum of 64k bytes of data that you may decide to locate in a piggyback EPROM. Software commands let you configure the direction of each chip's 44 I/O lines. A µPD78C1x with 256 bytes of RAM, 16k bytes of ROM, three timers, two zero-crossing detectors, and eight 8-bit A/D channels sells for \$6 (1000).

Outperform the standard

Even faster is Hitachi's 8-bit H8/532, which features a 0.2-µsec instruction-execution speed. In addition, the chip's CPU can run programs written in C. The development tool set includes an assembler, a C compiler, a software simulator/debugger, a hardware in-circuit emulator, and an evaluation board that you can use



For crash-proof operation, this 8-bit microcontroller from Dallas Semiconductor contains a built-in lithium-battery source. Another version includes an on-chip clock/calendar and nonvolatile RAM that allow your circuit to log events and schedule activities.



Look for a wide variety of packaging options, such as those available in Mitsubishi's 16-bit CMOS family of microcontrollers.

with an IBM PC or VAX workstation. The microcontroller has 29 built-in functions, including an A/D converter with a sample-and-hold device, a digital serial-communications interface, 1k byte of RAM, 32k bytes of EPROM, eight timers, and 65 I/O pins. Fabricated in 1.3- μ m CMOS, the one-time-programmable EPROM version sells for \$42.30 (1000).

Hitachi's HD647180X 8-bit microcontroller has a Zilog Z80-compatible architecture that lets you execute instructions in 0.375 µsec—twice as fast as Intel's 8051. The HD647180X directly executes existing Z80 programs with greater throughput; thus, you can use this microcontroller to speed your present designs, shrink a multichip design to one chip, or quickly develop high-speed communications applications. The chip comes with 15 peripheral functions, including two UARTs; three 16-bit timer channels; 54 I/O ports; an interrupt microcontroller; an analog comparator; a DMA microcontroller; and a memory-management unit (MMU). An 8-MHz version in an 84-pin, plastic leaded-chip carrier (PLCC) sells for \$19.10 (1000), or you can buy one EPROM version for \$99.

A chip for all reasons

Mitsubishi offers both variety and high performance in its 8-bit, CMOS microcontroller lines. Its Series 740 family of general-purpose, 8-bit, CMOS microcontrollers includes more than 70 masked ROM and ROMless versions; 15 piggyback development chips, eight with UV EPROM; and eight one-time-programmable ICs. Functions integrated on these microcontrollers include A/D and D/A converters; pulse-width modulation; LCD and vacuum fluorescent display drivers; 56 I/O ports; synchronous and asynchronous serial I/O; power-down modes; 3V battery operation; and master/slave opera-

Manufacturers of 8- and 16-bit microcontrollers

For more information on 8- and 16-bit microcontrollers such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Advanced Micro Devices

Box 3453 Sunnyvale, CA 94088 (800) 538-8450 (408) 732-2400 TWX 910-339-9288 Circle No 650

California Micro Devices

215 Topaz St Milpitas, CA 95035 (408) 263-3214 Circle No 651

Commodore Semiconductor Group

950 Rittenhouse Rd Norristown, PA 19403 (215) 666-7950 Circle No 652

Dallas Semiconductor Corp

4350 Beltwood Pkwy Dallas, TX 75244 (214) 450-0400 Circle No 653

Fujitsu Microelectronics Inc

Integrated Circuits Div 3545 N First St San Jose, CA 95134 (408) 922-9000 FAX 408-432-9044 Circle No 654

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Semiconductor and IC Div 2000 Sierra Point Pkwy Brisbane, CA 94005 (415) 589-8300 Circle No 656

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Intel Corp 3065 Bowers Ave

Box 58065 Santa Clara, CA 95052 (800) 548-4725 Circle No 658

MATRA-MHS

2840-100 San Tomas Expressway Santa Clara, CA 95051 (408) 986-9000 FAX 408-748-1038 Circle No 659

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Semiconductor Group 2191 Laurelwood Rd Santa Clara, CA 95054 (408) 980-4500 TLX 989791 Circle No 669

Signetics Corp

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Toshiba America Inc

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Vitesse Semiconductor 741 Calle Plano

Camarillo, CA 93010 (805) 388-3700 Circle No 673

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			UCTION (AVG)	LATENCY (CYCLES)	rs)	rh (BITS)	CE (BYTES)		end gerfans kee		(S	v,	V . 100 e4	VELS	RS	TIMERS	
COMPANY	MODEL #	# OF BITS	CLOCKS/INSTRUCTION (AVG)	INTERRUPT LA	АШ МЮТН (ВІТS)	DATA BUS WIDTH (BITS)	ADDRESS SPACE	RAM (BYTES)	ROM (BYTES)	EPROM (BYTES)	EEPROM (BYTES)	DMA#CHANNELS	MMU ON CHIP	INTERRUPT LEVELS	COUNTER/TIMERS	WATCHDOG TIN	
ADVANCED MICRO DEVICES	80C525/325, 80C521	8	8.75	3 TO 7	8	8	64k	256	8k	8k			1,3 3	2	2 (16 BIT)	1	
	8053	8	8.75	3 TO 7	8	8	64k	128	8k	8k				2	2 (16 BIT)	_	F-Million.
	80515/535	8	8.75	3 TO 7	8	8	64k	256	8k		_	_	_	4	3 (16 BIT)	1	
	80186	16	2 TO 67	1	16	16	1M	_	_	_		2	_	8	3 (16 BIT)	_	
CALIFORNIA MICRO DEVICES	G65SC150	8	3	8	8	8	64k	64	2k					3	2 (16 BIT)	_	
COMMODORE	6500/1	8	4	_	8	8	64k	64	2k		_	_	_	5	1 (16 BIT)	_	
DALLAS SEMI- CONDUCTOR	DS5000/ 5001	8	_	_	_	8		256 (NON- VOLATILE)	-	_	_	_	_		_	1	
Fujitsu	MB89710	8	4	4	16	8	64k×3	516	16k	16k	_	_	_	4	3	1	
	MB89730B/ 740B	8	4	4	16	8	16k	516	16k		-	-	_	3	3	1	
	MB89760	8	4	4	16	8	64k×3	516	16k	_	-	-	_	4	3	1	
HARRIS	RTX 2000	16	1	4	16	16	1M	2×512	-	-	-	5	YES	14	3 (16 BIT)	-	
	6805E3	8	12	12	8	8	64k	112	-	_	-	-	-	1	1 (8 BIT)	-	
	1805	8	10	10	1	8	64k	64	-	_	-	-	-	1	1 (8 BIT)	-	
	6805G2	8	10	10	8	8	64k	112	2106	_	-	-	_	1	1 (8 BIT)	-	
	68HC05D2	8	10	10	8	8	64k	64	2048	-	-	-		1	1 (16 BIT)	-	
HITACHI	HD647180X	8	6	17	8	8	1M	512	_	16k	_	2	YES	4 EXTERNAL 11 INTERNAL	2 (16 BIT)	_	
	HD6475328	8	4	18	16	16	1M	1k	-	32k	_	-	-	8	8	-	
	HD641016 CP-8/-10	16	4	48	32	16	16M	1024	_	_	_	4	_	3	2 (16 BIT)	-	
NTEL	87C51FB	8	12	4	8	8	128k	256	16k	_	-	0	0	2	3 (16 BIT)	1	
	80C196KA	16	6	2.5	16	16	64k	512	16k	_	_	0	0	-	6 (16 BIT)	1	
MATRA-MHS	80C31/ 80C51	8	12 TO 14	3	8	8	64k	128	4k	_	-	-	-	2	2 (16 BIT)	-	
	80C154/ 83C154	8	12 TO 24	3	8	8	64k	256	16k	_	-	_	-	2	3 (16 BIT)	-	
	78310A/ 78312A	16	6 TO 27	10	16	8	64k	256	8k		-	8		8	2 (16 BIT)	1	
MITSUBISHI	M37450M2/ M4/M8	8	-	16	8	8	64k	128/256/ 384	4k/8k/ 16k	-	-	-	-	15	4 (8/16 BIT)	1	

SERIAL PORTS	PARALLEL PORTS	A/D CHANNELS	D/A CHANNELS	UART ON CHIP	BIDIRECTIONAL LINES	SPECIAL VO DRIVERS	DEVELOPMENT TOOLS (M=MANUFACTURER'S T=THIRD PARTY'S)
1	4 (8 BIT)	_	_	YES	4 (8 BIT)	SLAVE INTER- FACE (525/325)	М,Т
1	4 (8 BIT)	_		YES	4 (8 BIT)	_	M,T
1	6 (8 BIT)	8 (8 BIT)	- 34 C	YES	6 (8 BIT)	` _	T.
_	-	-	_	NO	-	_	T
-	-	-		NO	27	2 SINE-WAVE GENERATORS	М
-	4	_	_	NO	4	INTERNAL PULLUPS	Т
-	-	-	_	NO	-	-	Т
1	53	8 (8 BIT)	2 (8 BIT)	YES	45	4 INPUT CAPTURE 4 OUTPUT CAPTURE	M,T
-	53	8 (8 BIT)		NO	21	24 VACUUM- FLUORESCENT- DISPLAY DRIVERS	M,T
2	69	8 (8 BIT)	2 (8 BIT)	YES	61	2 UP/DOWN COUNTER	M,T
_	1	- 2.2		NO	1 (16 BIT)		M,T
_	1 (8 BIT)	-		NO	1 (8 BIT)	_	М,Т
1		-	_	NO	1 (8 BIT)	_	М
_	1 (32 BIT)	-	_	NO	1 (32 BIT)	-	M,T
1	1 (28 BIT)	-		NO	1 (28 BIT)	_	M,T
2	_	6	-	2	54	HIGH-CURRENT PORT	M,T
1	65	8 (10 BIT)	· -	YES	8 (8 BIT)	LED, SCHMITT TRIGGER, INTERNAL PULLUPS	M,T
2	_	_	_	YES	_	-	M,T
1	4 (8 BIT)	0 A/D	0 D/A	YES	4	1	M,T
1	6 (8 BIT)	8 (10 BIT)	-	YES	3.5	3 PULSE-WIDTH MODULATORS, PERIPHERAL TRANS-SERVER	M,T
1	4 (16 BIT)	_		YES	4 (16 BIT)		Т
1	4 (16 BIT)	_		YES	4 (16 BIT)		Т
1	6 (16 BIT)	1 (8 BIT)		YES	6 (16 BIT)	2 PULSE-WIDTH -MODULATOR OUTPUTS	М
1	56	8 (8 BIT)	2 (8 BIT)	YES	40	_	M,T

tion. Minimum instruction-execution time varies from 1 to 2 $\mu sec.$

One of the newest members of the Series 740 family is the M37409M2 Intelligent Protocol microcontroller, which comes with 192 bytes of dual-port RAM and three full-duplex UARTs on chip. The microcontroller also has 320 bytes of RAM, 4k bytes of ROM, an 8-bit timer with a prescaler, and 16 I/Os. It costs \$9.75 (200). Suitable for facilitating multiprocessor communications, the microcontroller's serial-communication links let each μP perform a dedicated task in concert with the other processors in the system.

The M37450 family represents the high-performance side of the Mitsubishi 8-bit microcontrollers. These 10-MHz devices have a minimum instruction-execution time of 0.8 µsec. M37450 microcontrollers can also handle as many as 15 interrupts, allowing you to take advantage of a parallel-communication bus, three 16-bit timers, serial I/O, a UART, a stepper-motor control, and as much as 448 bytes of RAM and 16k bytes of ROM. The M37450M2, which has 4k bytes of ROM and 128 bytes of RAM, costs \$7.25 (5000).

Crash-proof your design

Other manufacturers' microcontroller families are proliferating, but Dallas Semiconductor seems to be practicing strict family planning. The DS5000 Soft microcontroller, introduced in 1987, has produced only two offspring: the DS5000T and the DS5001. The DS5000 begins with an Intel 8051 microcontroller core and adds nonvolatile registers and nonvolatile, static CMOS RAM, all powered by an embedded lithium source. The chip also comes with a power-fail warning interrupt, automatic power-down, and power-on restart functions; even if your circuit suffers a total power loss, the DS5000 not only won't crash, it will resume operation when power returns. The chip's softwareencryption logic, which uses a 40-bit keyword, protects your resident software from piracy. The DS5000 has 32 parallel I/O lines, a watchdog timer, serial I/O, and two 16-bit counter/timers. The microcontroller costs \$79.59 (100), and an evaluation kit sells for \$200.

The DS5000T lets you log events and schedule activities by time and date, thanks to its embedded clock/calendar. Prices start at \$64 (1000) for a version with 8k bytes of nonvolatile RAM. The DS5001 includes 128k bytes of nonvolatile RAM, improved software security based on a 64-bit keyword, and a destruct pin that causes the chip to develop amnesia if someone tampers with it. An 8042-style peripheral bus facili-

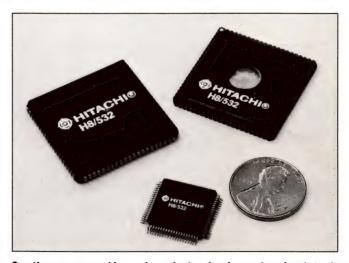
BLE 1—R	EPRESE	NIA	IIVE	8- F	AND	16-	BII	MICHC	COI	NIK	ULL	EKS	(C	ontinue	a)		Producer Code
COMPANY	MODEL #	# OF BITS	CLOCKS/INSTRUCTION (AVG)	INTERRUPT LATENCY (CYCLES)	ALU WIDTH (BITS)	DATA BUS WIDTH (BITS)	ADDRESS SPACE (BYTES)	RAM (BYTES)	ROM (BYTES)	EPROM (BYTES)	EEPROM (BYTES)	DMA#CHANNELS	MMU ON CHIP	INTERRUPT LEVELS	COUNTER/TIMERS	WATCHDOG TIMERS	
MITSUBISHI	MC68HC05B6	8	3	10 TO	8	8	8k	176	6k		256		_	6	1 (16 BIT)	_	
Continued)				21													
	MC68HC05C9	8	3	10 TO 21	8	8	16k	352	16k	-	_	_	_	6	1 (16 BIT)		
	MC68HC05L6	8	3	10 TO 21	8	8	8k	176	6k	-	-	_	-	5	1 (16 BIT)	-	
	MC68HC05P8	8	3	10 TO 21	8	8	8k	96	2k	_	16	_	-	4	1 (8 BIT)	-	
	MC68HC05U3	8	3	10 TO	8	8	4k	112	3.7k	AVAIL-	_	_	_	4	1 (8	_	
	MC68HC11E9/	8	4	21 12 TO	8	8	64k	512	12k	ABLE 12k	512	_	_	21	BIT) 2 (8/16	1	
NATIONAL SEMI- CONDUCTOR	711E9 COP8620C	8	1	52 7	8	8	32k	64	1k		64			3	BIT)	_	7.11828.00E
															BIT)		
	COP884CG	8	1	7	8	8	32k	192	4k	-		***************************************	-	14	3 (16 BIT)	1	
	HPC16003	16	2	31	16	16	64k	256					_	8	8 (16 BIT)	1	
	HPC16104	16	2	31	16	16	64k	512				-		8	8 (16 BIT)	1	
	HPC16400	16	2	31 2-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-	16	16	64k	256				4		8	4 (16 BIT)	1	
		ing ali bened			ostika (d	5 (2.5.1 h).			. Askazas	7 7 1 10 1 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	i dankaras	Sauce (Cons	and the same	katasi enda sa jangan samud	a ent de suit	Control of the Control	1×111/11/14/24
NEC	μPD78C1X	8	5	-	16	8	64k	256	16k	_	_			3	3 (8/16 BIT)	_	
	μPD7822X	8	2	-	8	8	64k	896	16k	_		6	_	2	3 (8/16 BIT)		
	μPD7823X	8	2		8	8	64k	896	16k	_	_	15	_	2	4 (8/16 BIT)	_	
	μPD7832X	16	2	_	16	8	64k	896	16k	_	-	8	-	3	8 (8/16 BIT)	-	
OKI SEMI- CONDUCTOR	MSM80C31/51	8	12	-	8	8	64k	128	4k	-			YES	5	2 (16 BIT)	_	
	MSM80C154/ 83C154	8	12		8	8	256	256	0/16k	and special to the second		-	YES	5	3 (16 BIT)	1	
	nXC66201/ 66P201	16	-		16	8	512k	512k	16k				YES	17	4 (16 BIT)	20 <u>-0.1</u> 43	
PHILIPS COMPONENTS	90C100/ 93C100	16	15	35	32	16	2M	512	0/34k	-	-	-	-	7	1 (16 BIT)	_	

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The state of the s	SERIAL PORTS	PARALLEL PORTS	A/D CHANNELS	D/A CHANNELS	UART ON CHIP	BIDIRECTIONAL LINES	SPECIAL I/O DRIVERS	DEVELOPMENT TOOLS (M=MANUFACTURER'S T=THIRD PARTY'S)
	1	32	1 (8 BIT)	2 (8 BIT)	YES	32	2 INPUT CAP- TURES, 2 OUT- PUT COMPARES	М,Т
	2	31	_	_	YES	31	_	М,Т
	1	24	-	_	NO	24	LCD DRIVER	M,T
	-	20	4 (8 BIT)		NO	16	_	M,T
	-	32	_	_	NO	24	-	M,T
	2	40	8 (8 BIT)	_	YES	16	8-BIT HANDSHAKE	M,T
	1	3 (8 BIT)		_		16	MICROWIRE/ PLUS, SCHMITT TRIGGERS	М
	2	23			YES	13	MICROWIRE/ PLUS, SCHMITT TRIGGERS, MULTI-INPUT WAKE-UP	X
	2	5 (8 BIT)	-		YES	32	MICROWIRE/ PLUS, 4 INPUT CAPTURES, UNI- VERSAL PERIPH- ERAL-INTER- FACE PORT	M,T
	2	5 (8 BIT)	8 (8 BIT)	- · · · · · · · · · · · · · · · · · · ·	YES	32	MICROWIRE/ PLUS, 4 INPUT CAPTURES, UNI- VERSAL PERIPH- ERAL-INTER- FACE PORT	M,T
	2	5 (8 BIT)			YES	32	MICROWIRE/ PLUS, SERIAL DECODER, 2- HIGH LEVEL DATA-LINK CONTROL CHANNELS	M,T
	1	5 (8 BIT)	8 (8 BIT)	_	YES	44	2 ZERO- CROSSING DETECTORS	M,T
	2	_	8 (4 BIT)	-	YES	71	MACRO SER- VICE, 2 REAL- TIME OUTPUTS	M,T
	2	-	8 (8 BIT)	2 (8 BIT)	YES	64	MACRO SER- VICE, 2 REAL- TIME OUTPUTS	М,Т
	2	_	8 (10 BIT)	- ;	YES	55	MACRO SER- VICE, CONTEXT SWITCHING, REAL-TIME PULSE	M,T
	1	32	-		_	32	FULL-DUPLEX SERIAL	М,Т
S. 1 &	1	32	-	_	YES	32		М,Т
	1	40	8 (10 BIT)		YES	40	2 PULSE-WIDTH MODULATORS	М
	2	2 (8/16 BIT)	-	_	YES	16	MULTIPLEXED 8051 BUS Table cor	 ntinued

tates intelligent peripheral control. The DS5001 costs \$125 (100).

Certain embedded applications require a greater focus on control than on speed. SGS-Thomson markets its ST6 family of 8-bit microcontrollers by touting the chips' ability to program I/O on either a bit or byte basis, and to program open-drain or push-pull I/O, as well as CMOS- or TTL-level input determination. Accordingly, you can program the 16 I/O pins for either digital or analog operation. The onboard, 8-bit A/D converter has 16 channels and an I²C bus speeds chipto-chip communications. The CPU is based on a 6804 architecture, and its small core draws as little as 2 mA for minimal power drain.

SGS-Thomson also offers an 8-bit, high-speed CMOS ST9 family, based on a CPU core derived from Intel's Z80 μP. The instruction set lets you program down to the bit level and utilize 14 addressing modes. Bytebased instructions execute in as little as 0.5 µsec. This family also comes with a multichannel DMA, a programmable interrupt microcontroller, and a real-time operating system. You can order versions with as much as 24k bytes of ROM or EPROM, 2k bytes of RAM, or 2k bytes of EEPROM. The MMU lets you address as much as 16M bytes of off-chip data. Peripherals include multiple 16-bit timers; a timing processor; a serial-communications controller; as many as eight parallel, 8-bit I/O ports; and an A/D converter. In addition, to help you combat noise problems, these devices let you shut down the high-current output pins when they aren't in use.



One-time-programmable versions shorten development cycles, but only if the EPROM device is pin compatible with the maskable version that you'll require once your production volumes increase.

				ES)							i					
COMPANY	MODEL #	# OF BITS	CLOCKS/INSTRUCTION (AVG)	INTERRUPT LATENCY (CYCLES)	ALU WIDTH (BITS)	DATA BUS WIDTH (BITS)	ADDRESS SPACE (BYTES)	RAM (BYTES)	ROM (BYTES)	EPROM (BYTES)	EEPROM (BYTES)	DMA#CHANNELS	MMU ON CHIP	INTERRUPT LEVELS	COUNTER/TIMERS	WATCHDOG TIMERS
PHILIPS	3349	8	1.3	5 TO	8	8	8k	224	4k	_	_	_	_	1	1 (8	_
COMPONENTS (Continued)	83/87C550	8	1.42	7 3 TO 8	8	8	4k	128	4k	4k		_	_	2	2 (16 BIT)	1
ROCKWELL INTERNATIONAL	R6500/12	8	3	3	8	8	16k	192	3k	-	-	_	_	10	2 (16 BIT)	-
INTERNATIONAL	R6500/15	8	3	3	8	8	16k	192	4k	_	_	_	_	10	2 (16 BIT)	_
	R65C119	8	3	3	16	8	64k	512	16k	-	-	_	-	10	4 (16/17	-
SGS-THOMSON	ST62XX	8	-	-	1	8	2k	64	2k TO 16k	-	32 TO 64	_	-	-	1 (16 BIT)	1
	ST63XX	8	52	_	1	8	2k	256	8k	_	128	_	-	5	2 (16 BIT)	1
	ST9	8	16	26	8	8	128k TO 16M	256 TO 128k	8k TO 128k			YES	YES	9	3 TO 5 (16 BIT)	-
	EF6805	8	5	11	8	8	-	64 TO 112	1100 TO 3776	-			-	3	1 (8 BIT)	-
SIEMENS	SAB8052	8	12	108	8	8	128k	256	8k	-	-	_	-	2	3 (16 BIT)	-
	SAB80512N	8	12	9	8	8	128k	128	4k	-	_	_	_	2	2 (16 BIT)	-
	SAB80C517N	8	12	9	8 Nedfer	8	128k	256	8k		- 		_	4	4 (16 BIT)	-
SIGNETICS	8051	8	12	3 TO 8	8	8	64k	64 TO 256	2k TO 16k	-	-	_	-	4 TO 15	1 TO 4	-
	68070	16	15	65	32	16	16M	EXTERNAL	EX- TER- NAL	27 <u>8.47</u> 28.68.61	19,025 19,025	2	YES		2 (16 BIT)	-
TEXAS INTRUMENTS	TMS370Cx50	8	8	15	8	8	112k	256	4k	AVAIL- ABLE	256	W.Z. 1		2	3 (16 BIT)	1
	TMS370Cx56	8	8	15	8	8	112k	512	16k	AVAIL- ABLE	512			2	3 (16 BIT)	4
	TMS70Cx2	8	8	17 TO 19	8	8	64k	256	4k	AVAIL- ABLE			75 <u>7</u>	1	3 (10/21 BIT)	1
TOSHIBA	TMP90C840	8	-	20	8	8	1M	256	8k	-	_	11	-	14	5 (8/16 BIT)	1
WAFERSCALE INTEGRATION	PAC1000	16	1	2	16	16	4M	64	_	8k	-	16	_	8	2 (22 BIT)	-
ZILOG	Z86C21/ Z86Z21	8	6	31	8	8	112k	236	8k	-	-	-	-	6	2	-
	Z8671	8	6	31	8	8	124k	124	-	-	-	_	_	6	2	
	Z8800 SUPER 8	8	-	_	_	_	128k	272	_	-	_	1	_	8	2 (16	_

	SERIAL PORTS	PARALLEL PORTS	A/D CHANNELS	D/A CHANNELS	UART ON CHIP	BIDIRECTIONAL LINES	SPECIAL VO DRIVERS	DEVELOPMENT TOOLS (M=MANUFACTURER'S T=THIRD PARTY'S)
		3 (4/8 BIT)				20	DTMF GENERATOR	М
	1	4 (8 BIT)	8 (8 BIT)	_	YES	24	_	М
	1	56	_	_	YES	14	-	М,Т
	1	32	-	-	YES	32	_	M,T
	1	58	-	_	YES	32	_	M,T
	1	2	16 (8 BIT)			16 (8 BIT)	PROGRAMMABLE OUTPUTS, INTER-IC	М
	1 34 1 2 4 TO 8 (8 7 (8 BIT) BIT) - 2 (8 4 (8		4 PULSE- WIDTH MODULA- TORS 1 14-BIT		34	PLL, LED, ON-SCREEN DISPLAY VOLTAGE SYNTHESIS	М	
			8 (8 BIT)		YES	4 TO 7 (8 BIT)	PROGRAMMABLE INPUT LEVELS, TOTEM-POLE OUTPUT	М
		— 2 (8 BIT)		-		2 (8 BIT)	_	M,T
	1	1 4 (8 BIT)		_	YES	4 (8 BIT)	_	Т
	1	7 (8 BIT)	_	_	YES	7 (8 BIT)	_	Т
	2	8 (8 BIT)	1 (8 BIT)		YES	9 (8 BIT)	21 PULSE-WIDTH MODULATOR OUTPUTS, 5 CAP- TURE INPUTS	Т
	1 TO 2	2 TO 7 (8 BIT)	5 TO 8 (8 TO 10 BIT)	1 OR 2 PULSE- WIDTH- MODULA- TOR OUT- PUTS	YES	2 TO 7 (8 BIT)	INTER-IC	M,T
	2	-	_	_	YES	_	INTER-IC	M,T
	2	5 (8 BIT)	8 (8 BIT)		YES	4 (8 BIT)	_	M,T
	2	5 (8 BIT)	8 (8 BIT)	_	YES	4 (8 BIT)	-	M,T
100	1	4 (8 BIT)		-	YES	3 (8 BIT)	The second secon	M,T
	1	54	6 (8 BIT)	8-BIT PULSE- WIDTH MODULA- TOR	YES	32	STEPPER-MOTOR CONTROL, 2- STAGE PIPELINED INSTRUCTION	M
	1	2 (16 BIT)	-	-	-	2 (16 BIT)		М,Т
		3 (8 BIT)			-	2 (8 BIT)	COMPARATOR	M,T
	1	4 (8 BIT)			YES	3 (8 BIT)	-	Т
	1	5 (8 BIT)			YES	5 (8 BIT)	-	Т

Acknowledging that the automotive and consumer markets are extremely price-sensitive, Zilog has debuted a family of low-cost, 8-bit microcontrollers called the Z86CXXCCP (Consumer Control Processor) Series. Ranging from \$1.50 to \$2.50 (10,000), these chips have a CMOS Z8 CPU core that operates over 2.5 to 5.5V. You can select versions that feature either 2k or 4k bytes of ROM; a 128-register file; brownout protection; a watchdog timer; on-chip analog comparators; two 8-bit counter/timers with a 6-bit prescaler; and halt and stop modes for low power consumption. You may also select an RC, ceramic, or crystal-oscillator circuit.

Texas Instruments has combined 512 bytes of EEPROM and 16k bytes of EPROM in its TMS370C756 CMOS 8-bit microcontroller. You can perform prototype or preproduction coding using the EPROM, which leaves the EEPROM available for system calibration or user-entered data. The TMS370C756 sample kit costs \$100. The company offers 15 other configurations in the TMS370 family at prices from \$5 to \$25.

As processing speeds increase and more functions are packed onto a single chip, the ruggedness of your microcontroller becomes more critical. National Semiconductor has taken steps to design safety margins into their double-metal M²CMOS devices. For example, the company's 8-bit COP800 microcontroller family offers fully static operation, features high ESD tolerance exceeding 2 kV, and functions over industrial and military temperature ranges. The inclusion of an epilayer in the fabrication process increases latch-up immunity. For even more security, you can purchase a version that has both a programmable watchdog timer and a nonmaskable software trap. Prices for the COP800 family start at 99 cents.

Is it 8 bits or not?

Fujitsu's interesting approach to boosting the performance of 8-bit CMOS microcontrollers is the use of a 16-bit core with an 8-bit data bus. The F²MC-8 family includes the usual assortment of on-chip peripherals and memory options at prices starting at approximately \$10 in OEM quantities. Instructions execute in a minimum of 0.5 µsec with an 8-MHz clock.

In contrast, Philips/Signetics has elected not to play favorites: Signetics bases its 8-bit microcontroller family on Intel's 8051 CPU, and the 16-bit microcontrollers Make sure that any prototype device you use matches the microcontroller with respect to form, fit, and function.

feature a CPU core derived from Motorola's 68000. Philips Components offers a selection that includes the Signetics microprocessors and adds several proprietary cores to the list. Signetics has announced a 28-pin, 80C51-based microcontroller called the 87C752 that includes an A/D converter and costs as little as \$3.

Siemens has recently introduced an 8051-compatible microcontroller that operates at 20 MHz. Fabricated in NMOS, the SAB 8032B lets you upgrade your 8031 or 8032 applications without a design change. The chip comes in a 40-pin DIP and costs \$4.96 (5000). It includes 32 I/O lines; three 16-bit timer/counters; a USART; 256 bytes of RAM; and a 6-source, 2-priority-level, nested interrupt structure. Another enhanced, 8051-compatible Siemens microcontroller, the SAB 80C157/80C537, lets you perform 16/32 bit arithmetic and provides indirect addressing of external memory through one data pointer. This CMOS microcontroller sells for \$24 (1000) and comes with two watchdog timers, 56 I/O ports, and two full-duplex serial interfaces.

Although 8-bit designs dominate the market, many developers have discovered that 16-bit CPU architectures offer higher throughput, more I/O, more timers, and support for high-level languages. For certain industrial-control applications—such as motor and motion control in hard-disk drives, high-speed communication devices, and laser printers—16-bit microcontrollers are indispensable.

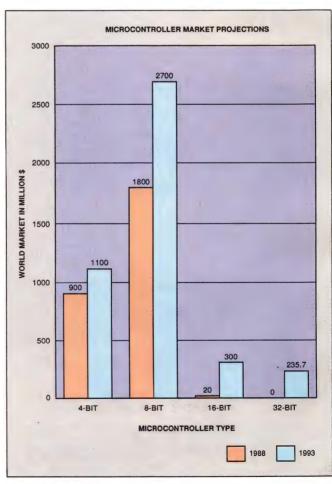
Just as Motorola is king of the 8-bit microcontroller market, Intel holds the lion's share of the 16-bit market. The company's premier product is the 80C196KA—a 12-MHz, CHMOS-III device that features 256 bytes of RAM, a pulse-width modulator, a 10-bit A/D converter, a serial I/O port, and five 8-bit parallel ports. The device comes in a 68-pin PLCC and costs \$18.75 (10,000). Improved throughput allows this microcontroller to perform a 3-operand multiply in 2.33

National Semiconductor maintains its number two position with its HPC family of 16-bit microcontrollers. Fabricated in double-metal CMOS, these chips operate at a clock rate of 30 MHz. The core includes an ALU, six registers, eight interrupts, three timers, control logic, a watchdog circuit, and a 16-bit-wide data path. The HPC family can address as much as 64k bytes of external memory. These chips use a proprietary instruction set optimized for maximum code efficiency. A typical instruction executes in 134 nsec, and a typical

16-bit multiply or divide takes less than 4 μ sec. You can also order a version with an embedded assembler in C code. The microcontrollers are priced from \$19.90 to \$39.50 (100).

Take a RISC for performance

Harris Semiconductor offers a remarkable 16-bit microcontroller that uses a Forth-based, reduced-instruction-set computer (RISC) core processor. The RTX 2000 features sustained performance exceeding 10 MIPS and directly executes the Forth language. Earlier this year, the vendor introduced the RTX 2001, which is pin compatible with the RTX 2000 but lacks the earlier device's single-cycle multiplier. Neverthe-



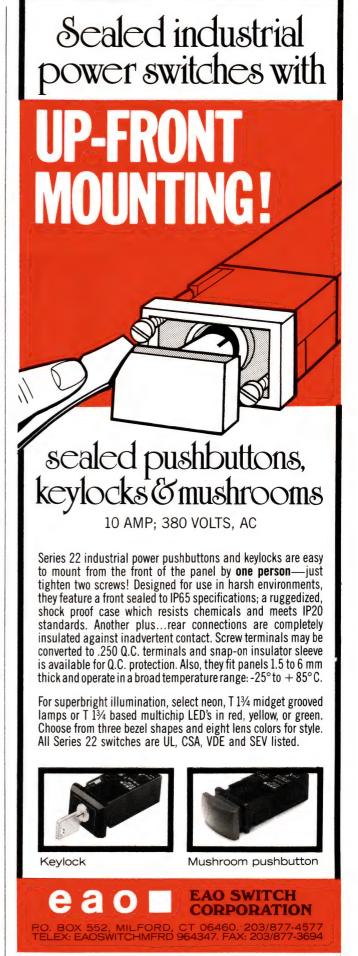
Although the 8-bit microcontroller market exceeds the current and projected dollar volumes for 16-bit microcontrollers, the higher profit margins keep manufacturers interested in expanding their 16-bit families. (Photo courtesy Integrated Circuit Engineering Corp)

less, the RTX 2001 performs multiply, divide, and square-root operations in approximately 2 μ sec. Both devices have two 64-word stacks on chip, a multiple-bus architecture, and a proprietary bus that lets you extend the chip's architecture by using off-chip, hardware-acceleration logic and application-specific I/O devices. The RTX 2000 costs \$190 (1000), and the RTX 2001 costs \$119 (1000).

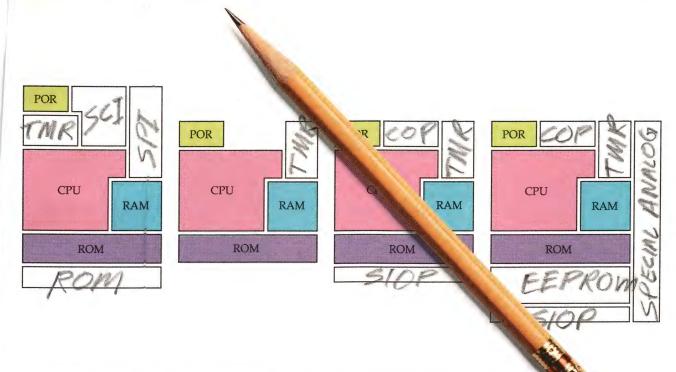
Waferscale Integration also offers a 16-bit, RISC-like microcontroller that uses parallel-processing techniques to boost performance. The PAC1000 contains 33 registers, a 15-word stack, and a $1k \times 64$ -bit EPROM. The PAC1000 is especially suitable for controlling peripheral devices that make rapid state changes, such as disk interfaces and multiprocessor bus-arbitration units. The microcontroller provides high-speed state control, computational functions, and memory-accessing capability. You program this microcontroller by using 64-bit words that include program control, CPU operation, and output control. Prices start at \$125 (100) for a 12-MHz version, or you can buy a 20-MHz chip for \$215.

Market projections for the next four years indicate that 8-bit chips will continue to reign in the microcontroller market. However, gross profit margins for 16-bit devices will represent 5% of all microcontroller sales, giving manufacturers the incentive to keep providing 16-bit families. As these manufacturers improve their processes and shrink die requirements, you can expect to gain even more power and performance from future microcontrollers.

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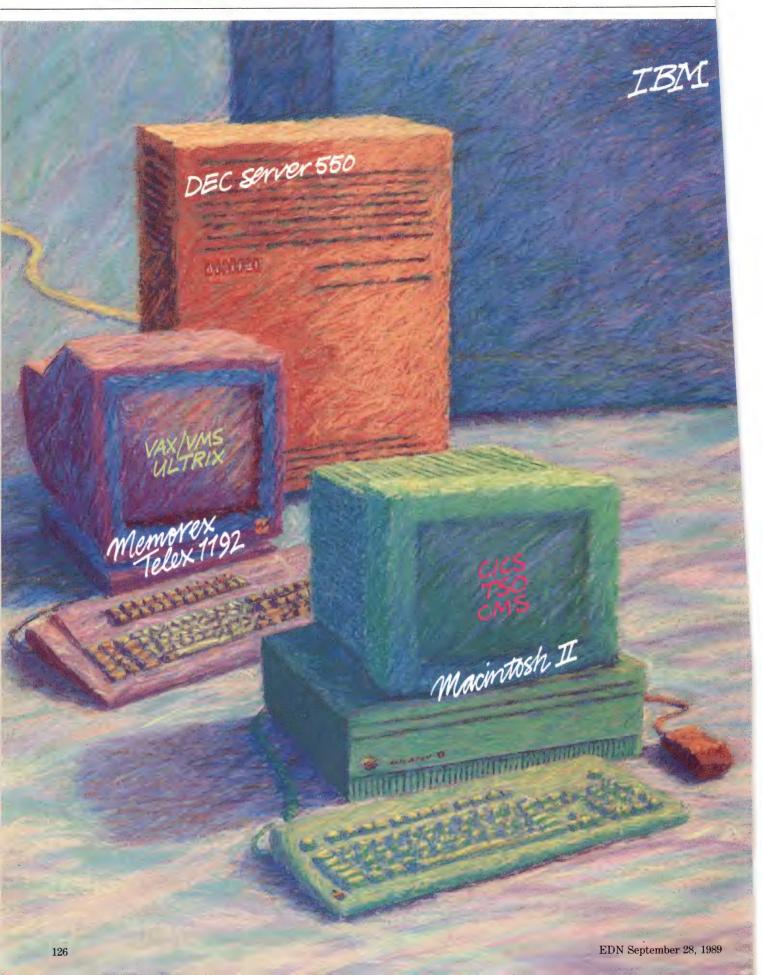
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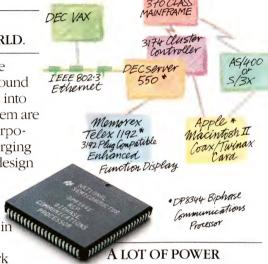
The DP8344 Biphase Communications Processor (BCP) is the key component in Apple's new adapter card for the Macintosh II—a landmark beginning in Apple's strategy of integration into the IBM mainframe environment.

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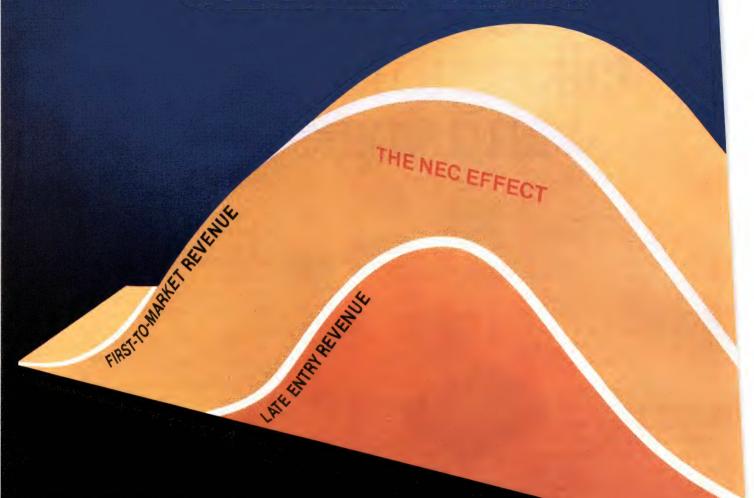
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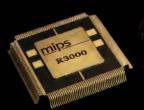
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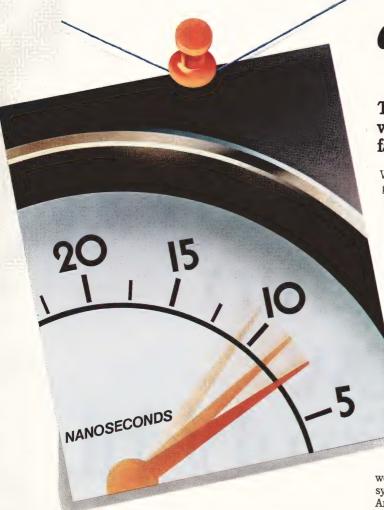
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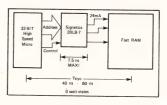
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microcontroller simulation Part 1

A simulator simplifies design verification of controller software

Design-verification tests aim to prove that your product will perform as specified and that hardware and software will work smoothly together, even under worst-case conditions. Part 1 of this 2-part article discusses some key issues (including the cost of testing) and shows how you can use a simulator to perform tests that would be difficult or impossible with standard hardware. Part 2 will presents a debugging example that shows how to simulate hardware that fails when you tell it to do so.

Anders Gezelius, Archimedes Software Inc

In a project's design-verification phase you normally test the final incarnation of the software as it executes on the completed target hardware (Fig 1)—but all too often, schedule and cost limitations prevent you from doing as much testing as you would like. When you're using real hardware, some types of tests are time-consuming (and therefore expensive); others involve such split-second I/O timing that you can never guarantee that you'll obtain the right conditions. A good simulator, however, can make such tests easy to set up and quick to execute, and it helps you lay to rest the nagging little voice in the back of your mind that keeps asking embarrassing questions such as

• What about those times the system hung and I never figured out why?

- Shouldn't I have tried the system with more than one of those new stepper motors?
- Did that last code change *really* solve the tricky timing problem I thought of?
- How much of the functional code have I actually exercised?

Manufacturing tests attempt to find errors in the assembly of an individual unit on the production line of a known-good product. By contrast, design-verification tests attempt to find out whether a correctly assembled unit will operate according to the specifications.

Routine tests of individual hardware subassemblies and software modules, which typically take place throughout the design process, go some way toward verifying individual parts of your design. The term "design verification," however, usually carries the connotation of a suite of system-level tests that you perform on the final product to make sure that all the parts work smoothly together. These final tests often involve checking system algorithms and timing under worst-case conditions to ensure that the system will never do anything that you don't expect. In particular, the system should handle all error conditions gracefully, giving the operator a chance to take corrective action.

Application determines the amount of testing

Most developers would agree that it is impossible to prove that a design is "correct," but most would also agree that testing for design errors is useful, beThe more a failure would cost, the more necessary it becomes for you to test for that failure.

cause additional testing almost always results in a better product. The problem is deciding how much testing to perform.

The cost of *performing* a test is relatively easy to estimate because equipment costs and engineering time are measurable. The cost of *not performing* a test is harder to estimate. If a problem is found later, how much will it cost to fix the units that have already been shipped? The direct cost depends on how large a change is required and how many units have been produced and shipped. Indirect and less tangible costs could result from impairment of your company's reputation if your product were to fail in the field.

In general, the more a failure would cost, the more valuable it is to test for that failure. For some products, such as medical instruments or process-control equipment, you may also have to consider the possibile legal ramifications of the damage caused by failure of the product. Of course, you also need to consider the probability of such a failure occurring.

Design-verification techniques cover a wide spectrum of cost and complexity. High-risk products warrant the use of expensive, special-purpose test equipment and custom-designed test systems (which are often more complex than the products they are designed to test). On the other hand, low-risk products may need little testing before being shipped (Fig 2).

If you're like the majority of developers, you operate somewhere between these two extremes. Although design errors in your product may not put lives at risk, field failures do generate direct repair costs for your company. Too many failures can give your company a bad reputation that results in lost sales, lower prices, and other consequences that cause revenue losses. For this intermediate group of developers, the cost and time required for testing are key factors in deciding how much design verification to perform. Design verification techniques must have a high return on investment—that is, they must cover many test cases at a relatively low cost per test.

Standard instruments vs simulation

Two approaches that yield a high return on investment are the use of standard hardware test equipment and software-debugging tools, and the use of simulators. If you take the hardware approach, you'll perform your design-verification tests on your final product with the aid of in-circuit emulators, pulse generators, oscilloscopes, and other equipment that is readily available in a typical development laboratory. Such tools let you perform a wide variety of tests, and you'll seldom need to purchase any extra, more specialized, equipment. However, you won't be able to begin design verification until you have a complete prototype of the target hardware.

Simulation can also provide a high return for your testing dollar. The cost of testing with a simulator is low, and a simulator often allows the execution of tests that would be technically difficult, or prohibitively time-consuming and expensive to perform on the actual hardware of the target system. Furthermore, a simulator that accurately models the timing of the microcontroller permits you to begin software-performance checks before the hardware is ready; if the simulator can also model the peripheral devices, you'll be able to get a good idea of how the whole system will perform. The test results may even reveal potential problems with the proposed hardware in good time for the

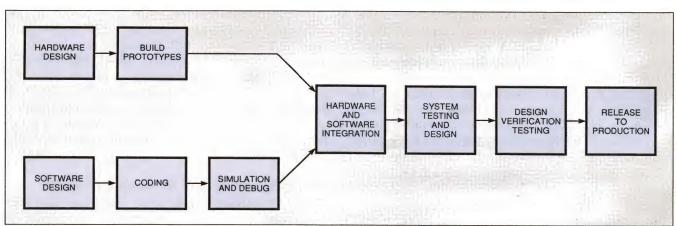


Fig 1—Design verification occurs at the end of the development cycle to ensure that the design is correct.

hardware designer to make the required modifications without incurring excessive costs.

Where simulation excels

A simulator is a powerful, yet economical, design-verification tool. Its ability to generate complex sequences of events makes it especially useful for tests in which random or infrequent events must occur in a known sequence in order to trigger the test case of interest. Because a simulator can simultaneously model events at varying levels of abstraction, an "event" could be something as simple as a transition on a signal wire, or something much more complex, such as an invalid parameter field in a command block passed between two processors.

Simulators are also good at generating test sequences that require very precise timing. This feature is useful for testing the operation of a system under worst-case conditions (when the hardware will operate at its fastest or slowest specified speeds).

Generating the stimuli required by a particular test is only half of the design-verification problem—observing the target system's response can be equally difficult, especially in microcontroller-based applications, because the response may be some change in the internal state of the microcontroller that is not immediately observable from outside the microcontroller. One of the benefits of simulating hardware is that the simulator can make internal hardware operations visible in a manner that would be impossible on the real hardware.

Both parts of this article will present examples of design-verification procedures that illustrate some of the capabilities of simulation. Each of the examples is based on the 8051 microcontroller, and each one in-

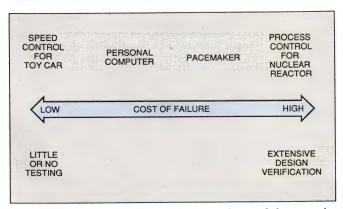


Fig 2—The cost of a failure determines the need for extensive design verification.



Running on an IBM PC or compatible, SimCASE uses multiple windows to provide many kinds of information during simulated execution of your software.

cludes a fragment of the operational code. For convenience, this code is written in Archimedes C, but the testing principles would be applicable to any code, regardless of the language (which might be PL/M-51, C for a different compiler, or assembly language).

The examples use the SimCASE Simulator/Debugger to perform the design-verification testing. SimCASE consists of an 8051 simulator with a convenient window-oriented debugger interface, which is indispensable during the early phases of software development.

Many simulators can model the processor chip itself; only a very few allow you to simulate individual hardware components (or even complete systems) that are external to the chip. SimCASE is one of these. It works with another software package, called SimI/O, which lets you model standard peripheral devices and allows you to create simulation models of any custom devices attached to your system. (See box "Overview of SimCASE and SimI/O" for background information about these two packages.)

Such extended modeling is crucial for design verification of microcontroller-based products, because many design-verification problems involve testing the response of the program to events outside the processor. As much as 90% of the operational code may be directly involved with controlling or sensing external hardware. The examples use SimI/O extensively to generate the stimuli needed by the tests and, more importantly, to simulate failures of the external devices. It's

Text continued on pg 136

Design-verification techniques should cover many test cases at a low cost per test.

SimCASE and SimI/O Overview

The Archimedes SimCASE Simulator/Debugger allows you to run and debug microcontroller code written in C, ASM, or PL/M. without hardware. The Archimedes SimI/O Simulation Toolbox allows you to test how your (SimCASE-simulated) microcontroller code responds to any types of I/O signals; you write simulation programs in Microsoft C-86 that model the I/O system of your application and link these programs to the SimCASE simulator.

SimCASE

The SimCASE Simulator/Debugger (8051 version) integrates a software simulator for the 8051 family of microcontrollers with a C-51 & PL/M-51 Source-Level Debugger and ASM Debugger. which are compatible with the Archimedes 8051 C compiler.

These software-development tools (Fig A) run on an IBM PC/ XT, PC/AT, or compatible com-

The Simulator Engine "executes" 8051 code by modeling the internal registers of the 8051 and then calculating the actions that would be taken by a real microcontroller for each instruction encountered. The simulator's model includes not only all of the CPU registers, but also the on-chip peripherals visible to the programmer, such as I/O ports, timers, serial port, and interrupt logic. The internal timing of the 8051 and all of its on-chip peripherals are modeled 100% accurately. permitting the simulation of realtime applications.

The C, PL/M, and ASM Debugger portion of SimCASE provides the user with a convenient, window-based interface to the simu-

lator. You can view program code at the source level-either as C or PL/M source code alone, or with the generated assembly language interspersed with the highlevel source statements, or in assembly language only (if the source module was written in assembly language). Debugger functions let you examine and modify the various internal registers and memory locations, using symbol names from the source code. You can execute code one step at a time, or run at top speed, halting at breakpoints that you've set at points of interest. A trace buffer provides a history of the instructions that have been executed so that you may inspect the sequence of events that led to a breakpoint.

A built-in Performance Analysis Tool generates graphic displays of execution data that the tool has gathered during simulation. Such data can help you analyze the performance of complex systems, identifying bottlenecks and unexecuted code blocks.

The debugger includes an Input Stimulus Generator, which allows you to model off-chip hardware designed into the target system. You can define input waveforms in a stimulus file and input these waveforms to the simulator during program execution. However, a stimulus file must be set up ahead of time and can't be changed during simu-

lation. SimI/O

The SimI/O package provides you with a flexible way to simu-

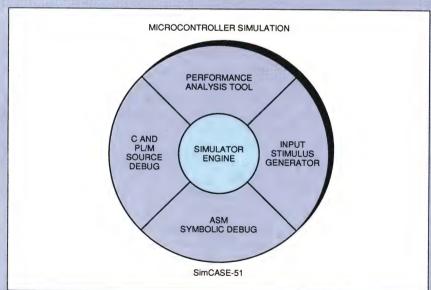


Fig A—SimCASE integrates a simulator engine with a source-level debugger, an inputstimulus generator, and a performance-analysis tool.

late the external hardware and the I/O signals that the microcontroller must handle. Because SimI//O is completely programmable, it's more flexible and powerful than the Input Stimulus Generator. For instance, you can send buffered live data via the IBM PC serial port to the SimCASE simulation. You can set conditional breakpoints on I/O ports, or any other memory location, using expressions in standard Microsoft C-86. You can also create easy-to-read timing-waveform diagrams, rather than reviewing trace buffers filled with zeros and ones.

How they work together

Fig B illustrates the overall relationships between your 8051 application, SimCASE, and the SimI/O Programs. Through the SimI/O Program interface, SIOPs (Simulated-I/O Programs) are closely coupled to the simulated 8051 "chip," to SimCASE, and to the program under test. An SIOP can monitor locations in the 8051 address space, including I/O ports, SFRs (Special Function Registers), external memory, and even internal memory. It may also modify any of these locations to provide adaptive or intelligent stimulus for the 8051 program being debugged. An SIOP may also time events in terms of the simulated 8051 clock.

It is this close coupling of an SIOP with the debug environment, combined with the flexibility of being able to code the SIOP yourself to perform almost any desired function, that gives

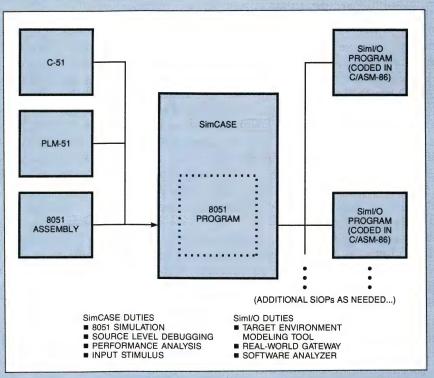


Fig B—SimCASE and SimI/O let you fully test 8051 code written in ASM-51, C-51, or PL/M-51, including the system response to I/O hardware malfunctions.

SimI/O its almost unlimited potential as a debugging and modeling tool.

Once an SIOP is mapped to an 8051 address, a 2-way interface is established between the SIOP and SimCASE. In one direction of the interface, SimCASE calls the SIOP whenever certain events occur-one such condition might be that an 8051 program writes to an address that is mapped to an SIOP. For each such event, there is a corresponding function within the SIOP; the function may contain user-written code to perform some action when the corresponding event occurs. These functions can perform tasks such as initialization, reset, termination, read, write, time delav, service request, reverse write, and keeping track of "reverse" time. A simple SIOP might use just one of these functions; a more complex SIOP might use them all.

In the other direction of the interface, the SIOP calls SimCASE when it wants to perform some function that only SimCASE can perform. For example, an SIOP can call SimCASE to read or write to any 8051 address or to perform a time delay in simulated 8051 time. The last part of the SimI/O interface is a global data structure that contains information about the state of SimCASE and the 8051 program it is running. It includes data elements that keep track of machine cycles, clock speed, chip type, (C-51) memory model and high-speed option status.

Simulation lets you perform tests that would be difficult or impossible to set up on the hardware.

difficult (and often impossible) to persuade a real peripheral to malfunction in the manner and at the exact time required in order to test the software's errorhandling capabilities.

Designing products that must respond intelligently to hardware failures can be quite difficult. Testing such products can also be difficult. You don't have to be designing a triply redundant flight-control system to be concerned about dealing with hardware failures—many products must react to hardware failures in a rational manner. For example, your product may have to turn on an indicator when the battery is low or blink out an error code when a peripheral chip doesn't respond to a command.

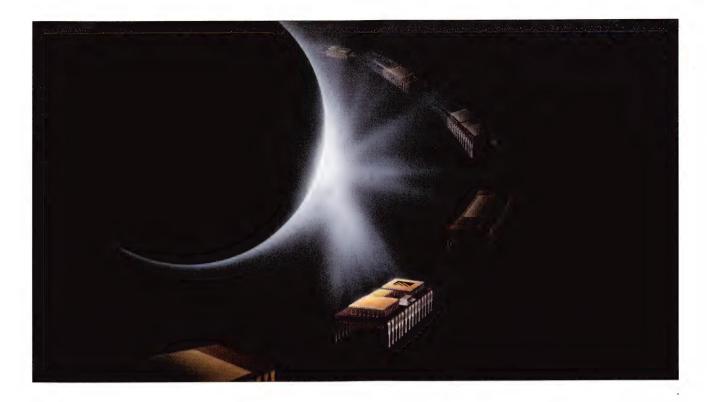
Such error handlers are a common source of design errors, because normal operation doesn't exercise them, nor do test procedures that are aimed at verifying correct normal operation. As a result, it is not uncommon for a simple, recoverable error to cause a system to hang. Unfortunately, error handlers can be especially tedious to test because they often contain a small, unique piece of code at each error-detection point to report the different types of errors and take the appropriate recovery action. For example, the code which handles a floppy-disk drive might respond differently to the following failures:

- A CRC (cyclic redundancy check) error in a sector's ID field
- A disk-drive motor that won't spin up at all (no index pulses)
- A disk controller that won't respond to any commands

Here, the differences in handling would probably be in the number of retries attempted and the action recommended to the user. The number of retries might vary from 0 to 100 and be different for each error. The action recommended to the user might be replacing the disk (in the first case); replacing the disk drive (in

LISTING 1—WALKING-1s RAM TEST

```
/**** Walking 1's RAM Test *****/
for (index = 0; index < 1024; index++) /* Clear all memory to 00 */
   write_XDATA(index, 0);
for (test_address = 0; test_address < 1024; test_address++)
     /* Test each of the bits in test_address */
   test_bit_mask = 0x80;
   while (test_bit_mask != 0)
         /* Test the bit selected by test_bit_mask */
      write_XDATA(test_address, test_bit_mask); /* Set test bit to 1 */
      /* Read and verify all memory locations */
      for (index = 0; index < 1024; index++)
         if (index == test_address)
              /* Verify data at test address */
               (read_XDATA(index) != test_bit_mask)
               display_RAM_fail(test_address, test_bit_mask, index);
         el se
               /* Verify data at other addresses */
            if (read_XDATA(index) != 0)
               display_RAM_fail(test_address, test_bit_mask, index);
      write_XDATA(test_address, 0);
                                    /* Clear test bit back to 0 */
      test_bit_mask = test_bit_mask >> 1;
   }
```



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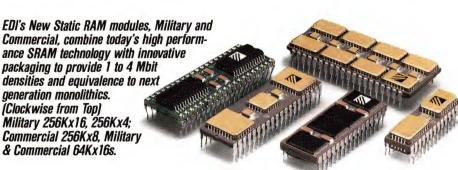
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Hardware that fails on command

The large number of cases that may require testing presents one kind of problem; but an even more difficult problem may be generating the failures that invoke the code to be tested. How do you force a disk drive to drop bits in a particular field of a sector? How do you force a status bit in a peripheral chip to "stick" at 0?

It's difficult enough to envision all the different ways that hardware can fail. To obtain samples of hardware that actually do fail in these ways may be nearly impossible. Simulation can provide a simple solution to the problem of how to effectively test your error-handling code. The symptoms of many types of hardware failure are much easier to produce with a simulator than with real hardware.

As an example, consider part of a self-test routine for an 8051-based product. This section of the self-test checks an external 1024-byte RAM, which the microcontroller uses as a data buffer during normal operation. The RAM test includes several test sequences to test for the following RAM failure modes:

- Addressability—the same location is accessed by different addresses
- Disturb failure—writing data to one location modifies data in another location
- Pattern sensitivity—some written patterns do not read back properly
- Retention failure—data can be read back correctly immediately after it has been written, but is corrupted after some period of time.

The test code shown in **Listing 1** performs a "walking-1s" RAM test to check for addressability and disturb failures. This code begins by writing 00 to all memory locations; then it sets the MSB of test≤bit≤mask to 1, writes this value to all locations, and reads all locations to ensure that they contain the proper value. The code then right-shifts the 1 into the next bit position of the test-bit mask, writes the new value to all locations, and again verifies the contents of all locations. It repeats this procedure until it walks the 1 into the LSB of the test-bit mask and checks each location.

In testing this code, there are two primary concerns: does the test actually detect RAM failures, and does it properly report them? The walking-1s test uses a "display≤RAM≤fail" function (not shown) to report a

LISTING 2—PROGRAM TO SIMULATE A FAILING RAM

```
unsigned int my_data;
 /* This function is called whenever the 8051 writes the SIOP's mapped address */
              word Data,
                          /* Data written by the 8051 program */
              byte Seg,
                          /* See siopInit */
              word Addr
                          /* See siopInit */
   my_data = Data;
   DATA_WRITE(Data, X_DATA_SEG, 33);
                                       /* Keep the write data */
                                      /* Write location 33, too */
/* This function is called whenever the 8051 reads the SIOP's mapped address */
            word *P_Data,
                              /* pointer to data to be read by the 8051 */
            byte Seg,
                              /* see siopInit, above */
            word Addr
  *P_Data = my_data;
  return OK:
```

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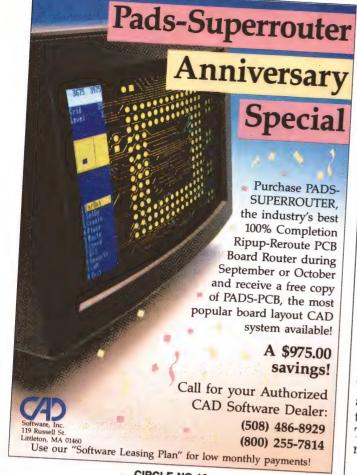
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CIRCLE NO 11

failure to the user on the product's console. This function could be sophisticated enough to try to analyze which component has failed. If so, it's important to check that the function selects the proper chip. On the other hand, even if this function only reports "The RAM has failed," it is important to ensure that it displays the correct message.

To test this code, you can write a very simple SIOP (Simulated-I/O Program) (Listing 2) to simulate a RAM that would fail a disturb test.

Because SimCASE, by default, effectively simulates a RAM at all external locations, the SIOP need only simulate the aberrant behavior of the failing location. To accomplish this, the "siopWrite" function intercepts all writes to the mapped location and writes the data to RAM location 33 as well as keeping a copy of it. This data is returned when the mapped location is read by the 8051 with the "siopRead" function.

Generating additional failure cases should be equally simple. To generate an SIOP that simulates a pattern-sensitive RAM, you would only need to test for a specific write-data pattern before modifying the stored data. Likewise, you could simulate a data-retention failure by requesting a time delay on every write operation to the mapped location. When the time delay expires, the SIOP could change the stored data.

Because the functions performed by these SIOPs are so simple, you could argue that it would be easier just to modify the simulated RAM contents manually (using the SimCASE Simulator/Debugger). Although this is true, you'll see in Part 2 that there are many advantages to creating tests that can be easily repeated without manual intervention.

Author's biography

Anders Gezelius is the president of Archimedes Software Inc, designers of software-development tools for microcomputers and microcontrollers. Anders holds an MS in electrical engineering from the Royal Institute of Technology in Stockholm, Sweden, and an MBA from the Wharton Business School in Philadelphia, PA. In his spare time he enjoys skiing, and he finds that studying world history is a humanizing counterbalance to the rigors of the technical world.



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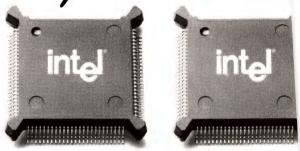
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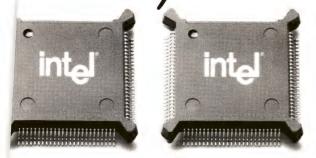
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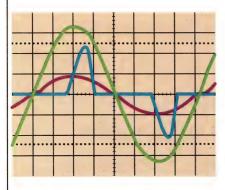
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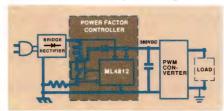
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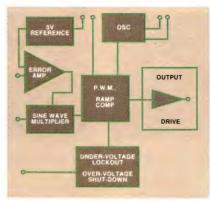
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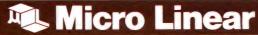
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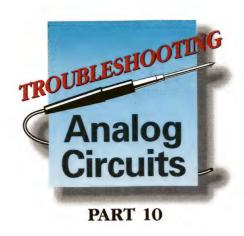
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The analog/digital boundary needn't be a never-never land

Past installments have dealt with circuit elements and circuits usually thought of as purely analog. Now Pease turns to an area that confounds and frightens all too many engineers—the boundary between the analog and digital worlds. Armed with a solid theoretical foundation and the insights presented here, you can keep your journey into the analog/digital world from seeming like a visit with Peter Pan.

Robert A Pease, National Semiconductor Corp

Many classes of circuits are neither entirely analog nor entirely digital. Of course, as an analog engineer, I don't have a lot of trouble thinking of *all* circuits as analog. Indeed, when problems develop in circuits containing both analog and digital elements, finding a solution is more likely to require that you summon your analog expertise than your digital knowledge. Timers, D/A and A/D converters, V/F and F/V converters, and S/H circuits all fall right on the boundary line between the analog and digital worlds. Digital ICs have more than a few analog subtleties. And even multiplexers, which you may have thought of as purely analog, have some quirks that result from their close association with the digital world.

A timer is basically a special connection of a comparator and some logic. The familiar 555 timer can do a lot of useful things, but it sure does get involved in a great deal of trouble. I'll treat the most classical fiascoes.

For one thing, people try to make timers with the crummiest, leakiest—usually electrolytic—capacitors. Then they complain because the timers are not accurate or their timing isn't repeatable. Some people insist on building timers to run for many seconds and then have trouble tweaking the time to be "exactly right." Sigh. These days I tell people, "Yes, you could make a 2-minute timer with an LM325 or a 10-minute timer with an LM322, but that would be WRONG." Instead, you could make a simple 1-Hz oscillator using one-quarter of an LM324 or LM339 and cheap, small components. This oscillator can drive a CD4020 or CD4040; the last output of that counter, $\div 2^{12}$ or $\div 2^{14}$, can time very accurately and conveniently.

Such an arrangement is cheaper and much more accurate and compact than what you get if you blow a lot of money on a 47-µF polyester capacitor for a long-interval timer, or put up with the leakages of a tantalum capacitor, which no manufacturer wants to guarantee. In addition, in just a few seconds, you can trim the moderate-frequency oscillator by looking at an early stage of the divider; trimming a long-interval timer can take hours. The CMOS counters are inexpensive enough, and these days for 2- to 20-minute timer applications, I can usually convince customers not to buy the linear part.

The LM555 data sheets tell you to avoid timing resistors with values higher than 20 M Ω . Nowadays, though, you can get a CMOS version (LMC555 or

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People try to make timers with the crummiest, leakiest—usually electrolytic—capacitors. Then they complain because the timers are not accurate.

equivalent) or use a CMOS comparator or a CMOS op amp to work at $100~\text{M}\Omega$ or more. Just be careful about board leakage and socket leakage—as you would with a high-impedance op-amp circuit. Then you can use a smaller, higher-quality capacitor.

Furthermore, it is a nontrivial statement that not all 555s work similarly; some manufacturers' 555s have different internal circuits and different logic flow charts. So be careful to check things out—555s from different manufacturers can act quite differently.

At high speeds, the timers don't just respond in a time $R \times C$; the response time is more like $R \times (C + C_{STRAY}) + T_{DELAY}$. Most books never mention this fact. So, although you can usually get a circuit to function, to get it to work the way you want it to, you still have to be careful. These designs are not always trivial, and **Ref 1** may help you avoid some pitfalls. A timer is, after all, just an aggregation of parts that includes a comparator, so many of the techniques you use with comparators work with timers and vice versa.

Digital ICs: not purely digital

Although timers are partly digital, the more classic digital ICs perform purely logical functions. Nevertheless, in the hands of a clever "linear" designer, some digital ICs can be very useful for performing analog functions. For example, CD4066 quad analog switches make excellent low-leakage switches and a 74C74 makes an excellent phase detector for a phase-locked loop (Ref 2). And not only is the price right—so is the power drain. Even when ordinary CMOS ICs aren't fast enough, you can often substitute a high-speed CMOS or 74ALS or 74AS counterpart to get more speed. I won't belabor the point; instead, I'll go straight to the litany of Troubles and Problems that you—whether an analog or a digital designer—can encounter with digital ICs.

First, unless proven otherwise, you should have one ceramic power-supply bypass capacitor in the range 0.02 to 0.2 μ F—or even 1 μ F, if the IC manufacturer requires it—for each digital IC plus a tantalum capacitor in the range 2 to 10 μ F for every two, three, or four ICs. The ceramic capacitors provide good high-frequency bypassing; the tantalum parts damp out the ringing on the power-supply bus. If you can't use a tantalum capacitor, you can try a 1- or 2- μ F extended-foil Mylar unit in series with a 1 Ω carbon resistor. If your linear circuit really depends on clean, crisp digital outputs (CMOS outputs make dandy squarewave generators, as long as the power supply isn't ringing and

bouncing) you may even want more bypassing—possibly hundreds of microfarads.

Floating inputs can leave you at sea

On TTL parts, you can leave an unused input floating and it will go high; on CMOS, you must tie unused inputs (such as the preset and clear inputs of a flip-flop) to the positive supply or ground, as appropriate. Otherwise, these inputs will float around and give you the screwiest intermittent problems. Also, when these inputs float, for example, on unused gates, they can cause considerable unwanted power drain and self-heating.

With CMOS, people keep telling you that you can use an inverter as an amplifier by tying a few megohms from the input to the output. At low voltages, you *can* make a mediocre amplifier this way, but when the supply voltage is above 6V, the power drain gets pretty heavy and the gain is low. I don't recommend this approach for modern designs.

Many years ago, people used to tie the outputs of DTL or open-collector TTL gates together to form a "wired OR" gate. This practice has fallen into disrepute as it supposedly leads to problems with troubleshooting. I don't know what other reason there is for not doing it except to avoid acting like a nerd. However, an open-collector output with a resistive pullup is slower than a conventional gate and wastes more power.

When digital-circuit engineers have to drive a bus for a long distance, say 20 or 30 inches, they use special layouts, so the bus will act like a 50Ω stripline. They also add termination resistors at one or both ends of the bus to provide damping and to cut down on reflections and ringing. When you have to drive long lines in an analog system, you should do the same. Note that for really fast signals, digital designers don't even lay out their pc traces with square corners; they bend the foil around the corner in a couple of 45° turns. Many digital engineers are not just bit-pushers; they've been learning how to handle real signals in the real world. They are actually pretty expert in some analog techniques, and analog engineers can learn from them.

Perfect waveforms don't exist

Even though many digital engineers are familiar with real problems, they often sketch the waveforms from gates and flip-flops showing nice, crisp, vertical rises and showing the output of a gate changing at the same time as the input. But smart engineers are aware

that when it comes down to the fine print, they must be prepared to admit that these waveforms have finite rise times and delays. These nit-picking details are very important when your signals are in a hurry.

For example, if the data input of a D flip-flop rises just before you apply the clock pulse, the output goes high. If the data input rises just after you apply the clock pulse, the output goes low. But if the D input moves at *just* the wrong time, the output can show "metastability"—it can hang momentarily half way between high and low and take several dozen nanoseconds to finally decide which way to go. Or, if the data comes just a little earlier or later, you might get an abnormally narrow output pulse—a "runt pulse".

When you feed a runt pulse to another flip-flop or counter, the counter can easily respond falsely and count to a new state that might be illegal. Thus, you should avoid runt pulses and make sure that you don't clock flip-flops at random times. Fig 1a contains an example of a D flip-flop application that can exhibit this problem. When the comparator state changes at random times, it will occasionally change at precisely the wrong time—on the clock's rising edge—making the output pulse narrower or wider than normal. In certain types of A/D converters, this effect can cause nonlinearity or distortion. A good solution is to use a delayed clock to transfer the data into a second flip-flop, as in Fig 1b.

A glitch is an alternate name for a runt pulse. A classic example of a glitch occurs when a ripple counter, such as a 7493, feeds into a decoder, such as a 7442. When the counter makes a carry from 0111 to 1000, for a few nanoseconds the output code will be 0000, and the decoder can spit out a narrow pulse of perhaps six to eight nanoseconds in duration corresponding to 0000. Even if you are observing with a good scope, such a pulse can be just narrow enough to escape detection. If the decoder were merely feeding an LED display, you would never see the submicrosecond light pulse, but if the decoded output goes to a digital counter, a false count can occur. In digital systems, engineers often use logic analyzers, storage scopes, and scopes with very broad bandwidths to look for glitches or runt pulses and the conditions that cause them. In analog systems, you may not have a logic analyzer, but these nasty narrow pulses often do exist, and you have to look for them.

Another thing to know about digital ICs is that many CMOS ICs have the same pinouts as TTL parts. For

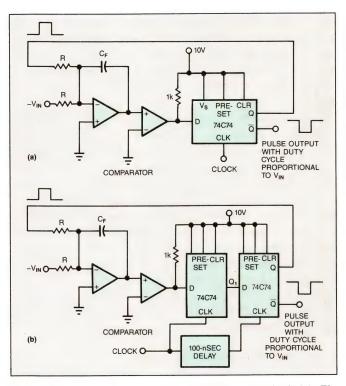


Fig 1—Runt pulses cause problems in this simple ADC (a). The comparator state changes at random times. Occasionally, the state will change at precisely the wrong time—on the clock's rising edge—making the output pulse narrower or wider than normal. You can solve the problem by using two flip-flops with the clocks separated by a delay (b).

example, the 74193, 74LS193, and 74C193 have the same pinouts. On the other hand, some of the older CMOS parts have pinouts that differ from those of similarly numbered TTL devices. The 74C86's pinout is the same as the 74L86's but differs from the 7486's. Beware!

Similarly, some CMOS devices have many—but not all—of their functions in common with those of their TTL counterparts. For example, the 74C74 has the same pinout and 98% of the same functions as the 7474. Both follow mostly the same truth table, except that when you pull both the preset and clear inputs low, the TTL device's outputs (Q and \overline{Q}) both go low, whereas the CMOS part's outputs both go high. If anybody has a complete list of such differences, I'd love to get a copy.

In some cases you can buy a buffered gate (CD4001BN), an unbuffered gate (CD4001), an unbuffered inverter (MM74HCU04), or a buffered inverter (MM74HC04). Sometimes, you can buy one part number and get an unbuffered part from one vendor

Digital engineers have been learning to handle real-world signals. They're experts in some analog techniques, and analog engineers can learn from them.

and a buffered one from another. Of course, the unbuffered parts are faster with light capacitive loads, but the buffered ones are faster with heavy loads. So if you have a critical application, be aware that substituting different vendors' parts can mess up your circuit.

Be careful when interfacing from linear ICs into digital ones. For example, an LM324 running on a single 5V supply doesn't have a lot of margin to drive CMOS inputs, but an op amp running on ± 5 or ± 10 V would need some kind of attenuation or resistive protection to avoid abusing the logic-device inputs (Fig 2). Likewise, it's considered bad form to overdrive the inputs of digital ICs just because they are protected by clamp diodes. For example, you can make a pulse generator per Fig 3, but it's considered bad practice to drive the inputs hard into the rail and beyond, as you will if the capacitance is more than 0.01 μ F or the power supply voltage is higher than 6V. The circuits in Fig 4 do as good a job without overdriving the inputs.

A time to ask probing questions

A number of years ago, I was watching the negative transition of an ordinary TTL gate, and I was especially concerned by the way it was overshooting to -0.4V. I set up an attenuator with 1 pF in the input leg (**Fig** 5), and was astounded to see that if I looked at the waveform with an ordinary (11-pF) probe, the

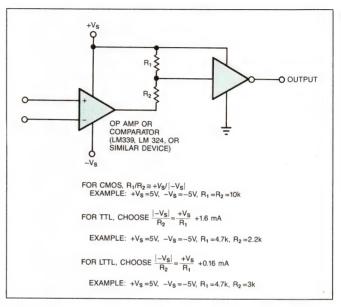


Fig 2—Driving logic from an op amp operating from the usual large supply voltages requires an attenuator between the amplifier and the logic IC. The equations show how to calculate the attenuator ratios.

overshoot occurred, but if I disconnected the probe from the gate output and connected it to the attenuator output, the overshoot went away. So, even if you use a fairly high-impedance probe, you should always be prepared for the possibility that by looking at a signal,

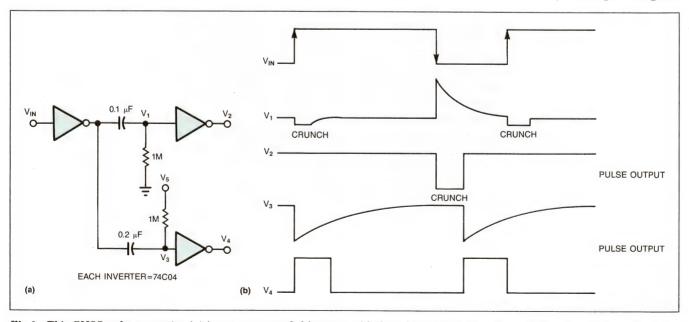


Fig 3—This CMOS pulse generator (a) is not recommended because, with the values shown, it overdrives the gate inputs excessively—as the waveforms of b indicate.

you can seriously affect it—even if what you're looking at is as mundane and supposedly robust as a TTL output. Consequently, you should be prepared to build your own special-purpose probes, so you can see what's really going on.

When I work with digital ICs, I would be easily confused if I did not sketch the actual waveforms of the ICs to show their relationships to each other. So I sketch these waveforms on large sheets of quadrule paper (½-in. grid) to produce something I call a "choreography" because it maps out what I want all the signals to do and exactly where I require them to dance or pirouette . . . When the system gets big and scary, I sometimes tape together two or three or four sheets horizontally and as many sheets as I need vertically. Needless to say, I am not very popular when I drag one of these monsters up to the copying machine and try to figure out how to make a copy. Fig 3b is a small example.

Maybe the guys who design really big digital ICs can get along without this technique; maybe they have other mnemonic tools, but this one works for me. I first developed this approach the time I designed a 12-bit monolithic ADC, the industry's first, back in 1975. I had this big choreography, about 33-in. square, and the circuit worked the first time because the choreography helped me avoid crossing up any digital signals. Right now I'm working on a system with one choreography in nanoseconds and tenths of nanoseconds linked to a second one scaled in microseconds and a third one scaled in seconds. I hope I don't get lost.

Of course, this tool is partly for design, but it's also a tool for troubleshooting—and for planning, so you can avoid trouble in the first place.

DACs are generally docile

DACs are pretty simple machines, and they can usually give excellent results with few problems. What kind of trouble can you get into with a DAC? If the manufacturer designed it correctly *and* you are not misapplying it, a DAC usually won't cause you much grief.

One area where DACs *can* cause trouble, however, is with noise. Most DACs are not characterized or guaranteed to reject high-frequency noise and jumps on the supply voltages. In some cases, the dc rejection can be 80 or 100 dB, but high-frequency noise on a supply can come through to the output unattenuated. So you must plan your system carefully. It might be

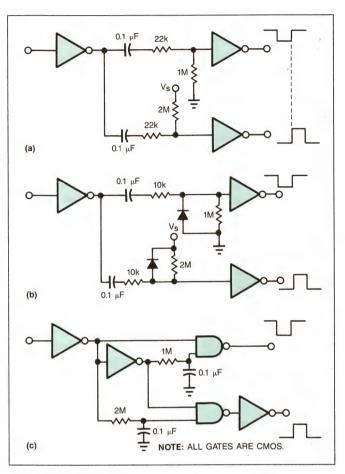


Fig 4—The addition of attenuators to the circuit of Fig 3 (a) helps reduce overdrive, but the addition of diode clamps in the shunt leg of the attenuators (b) is even more effective. If you have two 2-input NAND gates available, the circuit of c is the best implementation.

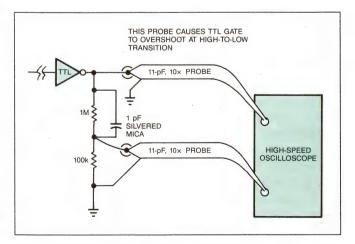


Fig 5—An ordinary high-impedance probe can cause TTL outputs to ring. You can eliminate this effect by cascading such a $10 \times$ probe with an attenuator of your own that presents a 1-pF capacitive load.

You should always be prepared for the possibility that by looking at a signal, you can seriously affect it.

a good idea to use a completely separate power-supply regulator for the DAC. At least you should add plenty of good power-supply bypass capacitors right at the power-supply pins—ceramic *and* tantalum capacitors.

Sometimes when you feed signals to a DAC without passing them through buffers, the noise, ringing, and slow settling of the digital signals can get through to the analog side and show up on the DAC output. Nobody has a spec for rejection of the noise on DAC bit lines in either the high or low state. Maybe vendors should specify this parameter, because some DACs are good and some aren't. I even recall a case where I had to preload the TTL outputs of a modular DAC's internal storage register. Otherwise they would overshoot when going high and then recover with a long slow tail, an attenuated version of which would appear on the DAC output.

On-chip buffers at a DAC's input can help cut down feedthrough from the bit lines to the analog output, but buffers usually can't reduce feedthrough from the data bus to the output. The bus can move around incessantly, and capacitive coupling or even pc-board leakage will sometimes cause significant crosstalk into the analog world. Even IC sockets can contribute to this noise. If you could prove that such noise wouldn't bother your circuit, you could forget about it. The problem is that you can only make meaningful measurements of such effects on an operating prototype—computer modeling can't simulate everything.

Multiplying DACs are popular and quite versatile. However, a multiplying DAC's linearity can be degraded if the output amplifier's offset voltage isn't zero. I've heard this degradation of linearity estimated at 0.01% per millivolt of offset. Fortunately, low-offset op amps are pretty cheap these days.

Another imperfection of any multiplying DAC is its ac response for different codes. If you put in a 30-kHz sine wave as the reference, you shouldn't really be surprised if the gain from the reference to the output changes by more than 1 LSB when you go from a code of 1000 0000 to a code of 0111 1111. In fact, if the frequency is above 5 kHz, you may find a 0.2% or larger error because the multiplying DAC's ladders, whose attenuation is a linear function of the input code at dc, become slightly nonlinear at high frequencies due to stray capacitance. The nonlinearity can be 0.2%, and the phase change as you vary the input code can exceed 2°, even with a 5-kHz reference. So don't let these ac errors in multiplying DACs surprise you.

Another problem with DACs is the output glitch

they can produce when going from one code to an adjacent one. For example, if a DAC's input code goes from 1000 0000 to 0111 1111 and the delay for the rising bits is much different from that for the falling bits, the DAC output will momentarily try to go to positive or negative full scale before it goes to a value corresponding to the correct code. Though well known, this problem is a specialized one. The solution requires precisely synchronous timing. Multiple storage registers can also help to save the day. If the best synchronous timing is not good enough, a deglitcher may be the solution.

ADCs can be tough and tempermental

Like DACs, many ADCs do exactly what they are supposed to, so what can go wrong? Most problems involve a characteristic that is mentioned on too few data sheets: noise. When an analog signal moves slowly from one level to another, it would be nice if the ADC put out only the code for the first voltage and then, at the appropriate threshold, began to produce only the code for the other voltage. In practice, there is a gray area where noise causes codes to come up when they shouldn't. On a good ADC, the noise can often be as low as 0.1 LSB p-p. But when you come to a worst-case condition (which with successive-approximation converters often occurs at or near a major carry—for example, where the output changes from 1000 0000 to 0111 1111), the noise often gets worse, sometimes climbing to 0.5 LSB p-p or more. I wouldn't want to buy an ADC without knowing how quiet it was. I'd have to measure the noise myself, as shown in Fig 6, because virtually nobody specifies it. That's not to say all ADCs are bad, just that manufacturers don't make much noise about noise.

Ron Knapp of Maxim wrote a nice explanation of an ADC noise measurement technique in EDN late last year (Ref 3). I recommend his article on this subject.

Most ADC data sheets spell out that the only correct way to test or use an ADC is with the analog signal's ground, the digital supply's ground, and the analog supply's ground tied together right at the ground pin of the ADC. If you don't or can't interconnect the grounds at the specified point, all bets are off.

With ADCs, paper designs aren't adequate

On one 10-bit ADC I designed, when the customer found some problems that I couldn't duplicate in my lab, I bought one plane ticket for me and one for my best scope. After a few hours we arrived at the scene,

and in less than an hour I had the problem defined: The customer expected our converter to meet all specs with as much as 0.2V dc plus 0.2V ac, at frequencies as high as 5 MHz, between the analog ground and the digital ground. Amazingly, our architecture was such that by deleting one resistor and adding one capacitor, I could comply with the customer's wishes. Most ADCs couldn't have been made to work—the customer was

fantastically lucky that I had used a weird design that was amenable to this modification. My design was a high-speed integrating converter with an input voltage-to-current converter that just happened to be capable of rejecting wideband noise and dc offsets between grounds.

The general lesson is that any ADC system is nontrivial and should be engineered by actually plugging in

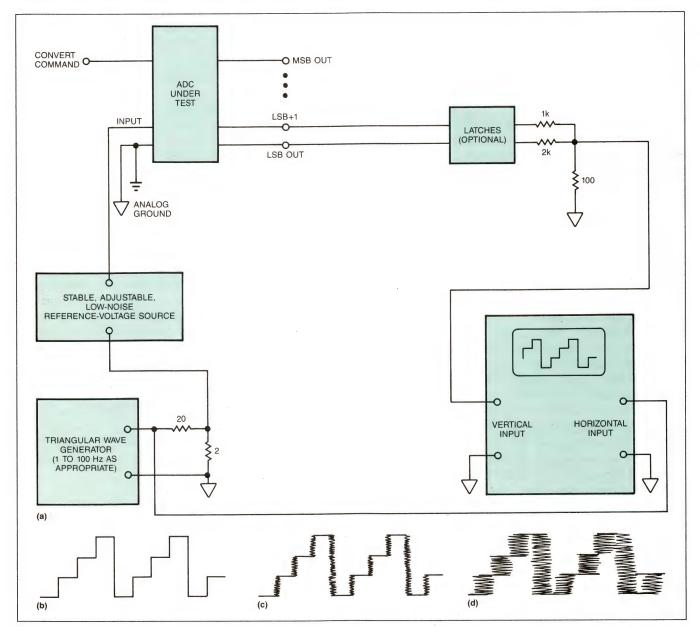


Fig 6—A reference source, a triangular-wave generator, and a scope are the major building blocks of an ADC crossplot tester (a) that can reveal how much noise a converter adds to the signal it is digitizing. In b, the noise performance is ideal, whereas in c, it is merely acceptable. In d, the noise performance is unacceptable.

Most DACs are not characterized or guaranteed to reject high-frequency noise and jumps on the supply voltages.

some converter circuits. "Paper designs" usually don't hold water in ADC systems.

To beat the requirement that every ADC have its own set of power supplies dedicated exclusively to powering just the single converter, you may want to bring power to your pc boards in unregulated or crudely regulated form and put a small regulator right near each ADC. These small regulators (whether LM320, μ A7800, LM317, or whatever) do *not* have a high power-supply rejection ratio at high frequencies. You can resolve that problem with decoupling, so you have a chance to make the scheme work. I hasten to point out, however, that I haven't actually built such a system myself.

Don't let ground loops knock you for a loop

The need for multiple power supplies, or at least multiple regulators, comes, of course, from the many paths taken by ground currents flowing to and from the power supplies. If you don't keep these paths scrupulously separate, the ground loops can cause bad crosstalk between various parts of the system—low-level analog, high-power analog, and digital. So be very careful to avoid ground loops when you can. Although the electrical engineering faculty at your local university might not agree, a general solution to the ground-loop problem would be an excellent subject for a PhD thesis. If you write such a dissertation, please don't forget to mail me a copy.

Some successive-approximation ADCs have separate buffers feeding their output pins, but other designs try to save money, parts, power, or space by using the internal registers to drive both the internal DAC and the output pins. In this case, external loads on the outputs can cause poor settling and noise and can thus degrade the performance of the converter. If you're using ADCs, you should find out if the outputs are connected directly to the DAC. Sometimes, as previously mentioned, preloading the bit outputs helps to accelerate settling of an ADC's internal DAC. After all, TTL outputs must be able to drive more current than their dc specs state—they have to meet their ac specs.

VFCs and FVCs frequently find favor

The voltage-to-frequency converter (VFC) is a popular form of ADC, especially when you need isolation between the analog input and digital outputs. You can easily feed a VFC's output pulse train through an optoisolator. The VFC can cover a wide range with 14 to

18 bits of dynamic range. The less expensive VFCs are slower; the faster ones can be expensive. Most VFCs have excellent linearity, but the linearity depends on the timing capacitor having a low dielectric absorption. Teflon makes the best VFC timing capacitors, but polystyrene, polypropylene, and ceramic capacitors with a COG characteristic are close behind.

Trimming a VFC to get a low temperature coefficient is not easy because the overall temperature coefficient depends on several components, including the reference, as well as various timing delays. See **Ref** 4 for VFC trimming procedures or, at least, to appreciate how much effort is involved when you buy a well-trimmed unit.

Frequency-to-voltage converters (FVCs) are often used as tachometers or in conjunction with a VFC and an optoisolater to provide voltage isolation in an analog system. FVCs are about as linear as VFCs and about as drifty, so the temperature trimming problem is the same as for a VFC. One exception is if you're using cascaded VFC/FVC pairs in which both circuits are in the same location and at the same temperature. In that case, you can often get by with trimming only one of the pair.

Another problem with FVCs is that you often want the response to be as fast as possible but need to keep the ripple low. The design of a filter to accomplish both objectives will, of course, be a compromise. My rule of thumb is that you can keep the ripple down to about 0.01% of the $V_{\rm FULLSCALE}$, but with the simplest filters, you must keep the carrier at least 100 times the $F_{-3~\rm dB}$. With more sophisticated filtering, such as two Sallen-Key filters cascaded, the -3-dB point can be $\frac{1}{10}$ of the slowest carrier. For example, with a carrier frequency in the range 5 to 10 kHz, the signal can go from dc to 500 Hz (Ref 5). If you need still faster response, see Ref 2, which shows how to use a phase-locked loop to make a quick FVC.

S/H circuits: electronic stroboscopes

A VFC produces an output proportional to the average value of its analog input during the conversion. If you need to digitize rapidly changing signals, for example, to reconstruct waveforms in the digital domain, you need a different type of ADC and you almost always have to precede it with a sample-and-hold circuit. Designing S/H circuits is a complicated, challenging endeavor. Meeting exacting specs often requires an expensive module or hybrid circuit. A major problem of S/H circuits is dielectric absorption, or "soakage,"



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On-chip buffers at a DAC's input can help cut down feedthrough from the bit lines to the output but usually can't reduce feedthrough from the data bus to the output.

in the hold capacitor (Ref 6).

If you need to run a relatively short sample time with a long hold time and if the new output voltage can vary considerably from the previous sample, the soakage may be your biggest problem. For example, if an S/H circuit acquires a new voltage for 5 µsec and then holds it for 500 µsec, you can tell approximately what the previously held signal was because the new V_{OUT} can shift by 2 to 3 mV—the amount and direction depend only on the value of the previous signal. And that's for an expensive Teflon hold capacitor-most other capacitors have soakages three to five times worse. If the timing doesn't change, you may be able to add a circuit to provide some compensation for the soakage (Ref 7); but the problem isn't trivial, and neither is the solution. Cascading two S/H circuits—a fast one and a slow one with a big hold capacitor-won't help the soakage but will tend to minimize the problem of leakages.

Some people wish that a S/H circuit would go from sample to hold with a negligible jump, or "glitch." Although you *can* build such a circuit, it's a lot more difficult than building a more conventional S/H circuit. You usually find glitch-free S/H circuits only in "deglitchers," which are more expensive than most S/H circuits. Several module and hybrid manufacturers provide this kind of precision device. Even though it doesn't settle out instantly, a deglitcher is fast and consistent in its settling. However, it still does take some time to settle within 5 mV.

Aperture time still causes confusion

There's one area of specsmanship where the S/H circuit is clouded in confusion. That area is the aperture-delay specification. (Maybe someday I'll write a data sheet and drive away the cloud.) One technique for measuring and defining aperture delay is to maintain $V_{\rm IN}$ at a constant level and issue the hold command. If after a short delay, $V_{\rm IN}$ jumps by a few volts, the smallest spacing between the hold command and the $V_{\rm IN}$ jump that causes no false movement of $V_{\rm OUT}$ is one possible definition of the $t_{\rm APERTURE}$ Delay.

Another way of defining and measuring aperture delay might be to let $V_{\rm IN}$ move smoothly at a well-defined rate. Shortly after you issue the command to switch the circuit to the hold mode, $V_{\rm OUT}$ stops changing. The value at which $V_{\rm OUT}$ stops corresponds to the value of $V_{\rm IN}$ at a particular point in time. You can define the aperture delay as the difference between this point and the point at which the mode-control



Pease irritates coworkers when he carries one of his "choreographies" to the photocopier and tries to figure out how to duplicate such a large drawing.

signal crossed the logic threshold. The uncertainty in the value of the aperture delay is then the aperture uncertainty. Depending on how the circuit was optimized, that delay can be positive *or* negative *or* practically zero—perhaps only 1 nsec or less. Now, will the *real* definition of aperture time please stand up?

I think that both of the characteristics I have described are of interest to people at different times. But, how can you avoid the problem of a person expecting one of these characteristics and actually getting the other? I invite your comments on who wants to buy which characteristic, and where to find a definition. I've looked in military specs and at many data sheets, and the issue still seems pretty unclear.

Another instance in which a S/H circuit can have trouble is when its output is connected to a multiplexer, for example, when multiple S/H circuits drive a single ADC to achieve simultaneous sampling of many channels of dynamic analog data. If the multiplexer, which had been at a voltage of, say, 10V; suddenly connects to the output of a S/H circuit whose output is at -10V, the circuit's output will twitch and then jump to a false level because the multiplexer will couple a little charge into the hold capacitor. The industry-standard LF398 is fairly good at driving multiplexers, but if you get a big enough capacitor and it's charged to a voltage 20V away from the S/H circuit's output voltage, even the LF398's output can jump. I don't have a real solution for this problem, but if you are aware that it can happen, at least you won't tear out all your hair trying to guess the cause. You will recognize the problem,

otographs by Pegai Willis

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standards, is compatible

Any ADC system is nontrivial and should be engineered by actually plugging in some converter circuits. "Paper designs" usually don't hold water in ADC systems.

and *then* tear out your hair. About all you can do is try to minimize the capacitance on the output of the multiplexer. One way to do this is by using a hierarchical connection of submultiplexers.

No agreement on acquisition time's meaning

Another area of S/H-circuit confusion is acquisition time. I have seen at least one data sheet that defined acquisition time as the time required to go from hold to sample and for the output to settle to a value corresponding to a new value of $V_{\rm IN}$ in the sample mode. However, the outputs of many S/H circuits can settle to a new dc value faster than the hold capacitor charges to the correct value. To avoid confusion, I define acquisition time as the pulse width required for precise sample-and-hold action. If the circuit samples and settles and then goes into hold and gives you the wrong answer, the sample pulse should have been wider.

There may be some S/H circuits whose output voltage won't change if you switch them to the hold mode as soon as their output reaches a value that corresponds to a new $V_{\rm IN}$. But if I had an analog switch that couldn't hold at all, I could still get it to "acquire" a signal according to the data-sheet definition just cited. I consider the test implied by that definition to be too easy. I believe some users and manufacturers in this field agree with my definition, but the situation isn't really clear. (I would appreciate reader comments. You folks are getting all sorts of good ideas from me, and if you have some good comments, it's only fair that you bounce them off me.)

E pluribus unum: the multiplexer

Another type of circuit that depends on analog switches is the analog multiplexer. As mentioned already, a multiplexer can draw big transients if you suddenly connect it across big signals at low impedances. So be careful not to overdo operating a multiplexer in this manner, as excessive current could flow and cause damage. It's well known that multiplexers. like most other forms of analog switches, are imperfect due to leakages, on-resistance, and response time. But they are popular and won't give you much trouble until you turn the power bus off and keep the signals going. I recall that in the past few years, at least one or two manufacturers have brought out new designs that could survive some fairly tough overvoltages with the power removed. I'm not sure what the designs involved other than adding thin-film resistors and diode clamps on the inputs—ahead of the FET switches. But if you add discrete resistors ahead of a multiplexer's inputs, the resistors can help the multiplexer survive the loss of power.

One other problem with multiplexers is that you don't have a whole lot of control over the break-beforemake margin. And if you should want make-beforebreak action, I don't think it's an available option. So, sometimes you may have to "roll your own" multiplexer.

If your signal levels are less than 15V p-p, you may be able to use the popular CD4051 and CD4053 multiplexers and the CD4066 CMOS analog switches, which are inexpensive and quick and usually exhibit low leakage. However, if you need a guarantee of very low leakage, you may have to test and select the devices yourself.

So, we take leave of the analog/digital world—sort of. Next time, we'll visit another area of great importance to analog/digital electronics, but it is a purely linear region, perhaps the *most* purely linear: references. Armed with knowledge about references, we'll move on to the troubleshooting of power electronics, including switching regulators.

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Author's biography

For more information on Bob Pease, see the **box**, "Who is Bob Pease, anyway," on page 148 of the January 5, 1989, edition of EDN.

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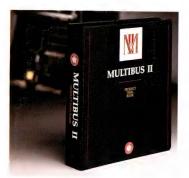
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DESIGN IDEAS

EDITED BY CHARLES H SMALL/ANNE WATSON SWAGER

Transistors boost difference amp

R Mark Stitt and Rod Burt Burr-Brown Co, Tucson, AZ

Adding a few cents worth of garden-variety parts to an INA105 difference amplifier's circuitry enables it to provide nearly a full $\pm 15 \mathrm{V}$ output swing from a $\pm 15 \mathrm{V}$ supply. Difference amplifiers have a high input common-mode range. Their inputs can accept signals that swing beyond both power-supply rails by up to $5 \mathrm{V}$; unfortunately, most such amplifiers guarantee output swings of only ± 10 or $\pm 12 \mathrm{V}$ from a $\pm 15 \mathrm{V}$ supply.

Fig 1 shows the modified difference-amplifier circuit. The sum of the amplifier's quiescent current and the output current flowing through its power-supply pins drives external transistors Q_1 and Q_2 through base-emitter connected resistors R_3 and R_4 . Q_1 and Q_2 are common-emitter amplifiers and provide a gain of approximately 1.7. Thus, the amplifier's output needs to swing only about $\pm 9V$ to obtain a $\pm 15V$ swing at the buffer's output. Fig 2a shows that this circuit avoids crossover distortion—a common bugaboo of boosted amplifiers.

Even though the amplifier's feedback circuit provides gain, the scope photo in Fig 2b shows that the small-signal response of the circuit remains stable. Because a difference amplifier operates with a noise gain of two, you can add gain in its feedback loop without causing instability if you hew to the following three rules: The added gain must be less than two, the op amp in the difference amplifier must be unity-gain sta-

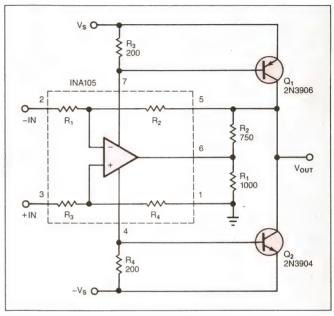


Fig 1—External transistors Q_1 and Q_2 boost the output of the difference amplifier so that it can swing close to the voltage-supply rails.

ble, and the phase shift added though the gain network must be small at the unity-gain frequency of the difference amplifier's op amp.

This circuit meets these requirements. A block diagram of the composite amplifier (Fig 3a) illustrates the circuit's feedback loops. Resistors R_1 and R_2 set the gain of the buffer amplifier, A_2 , which is a current-feedback op amp formed from the output transitors in

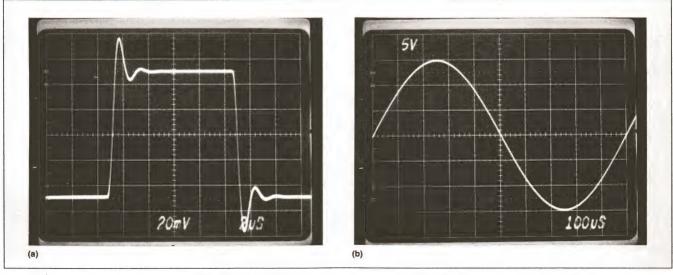


Fig 2—The scope photo in (a) shows that the circuit's response to a sine-wave input has no crossover distortion. The scope photo in b shows the stable small-signal response of the circuit driving a 100-pF load.

EDN September 28, 1989

DESIGN IDEAS

the difference amplifier and the external transistors. Current-feedback amplifiers are known for their wide bandwidths and low phase shifts (Ref 1).

Fig 3b shows one of the two complementary currentfeedback amplifiers formed from the NPN transitor in the output stage of the difference amplifier and PNP external transistor Q_1 . This portion of the circuit is active for positive output swings. The complementary section, which uses Q_2 , is active for negative swings.

A word of caution: To obtain the extra swing, this design sacrifices output-protection circuitry. The out-

put buffer has no current limiting, so a short circuitat the output could destroy one of the external transistors.

Reference

1. Franco, Sergio, "Current-feedback amplifiers benefit high-speed designs," *EDN*, January 5, 1989, pg 161.

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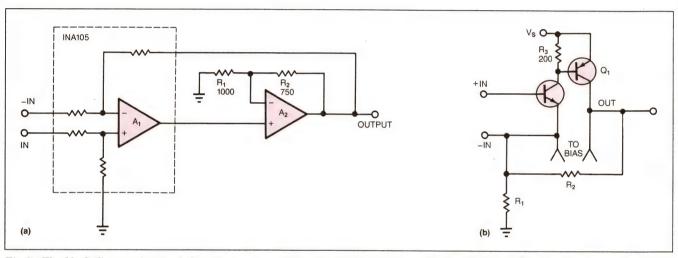


Fig 3—The block diagram in a and the equivalent circuit of one-half of the symmetrical output stage in b illustrate the feedback scheme of the difference-amplifier circuit.

Program generates pseudonoise

Thom Van Nguyen Qualcomm, San Diego, CA

A program, available in Basic and Pascal versions, permits a computer to simulate the function of a hardware pseudorandom-pattern, or pseudonoise, generator. The program will first ask you to supply a value for n between 2 and 35. The program uses this value to set up a software model of a standard 2^{n-1} stage shift register with exclusive-OR (XOR) feedback of one of the stages (**Fig 1**). Such feedback shift registers are called pseudorandom generators because they repeat their pseudorandom patterns every 2^{n-1} bits.

You can select one of two feedback configurations depending on the value of n. If n is odd, the program will XOR the second and final stages; if n is even, the program will XOR the final two stages.

The program will display the generator's bit stream in binary and hex. You can use the program to evaluate pseudorandom-pattern generators of various lengths

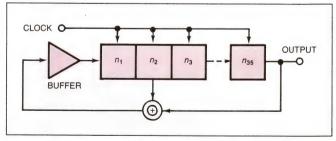
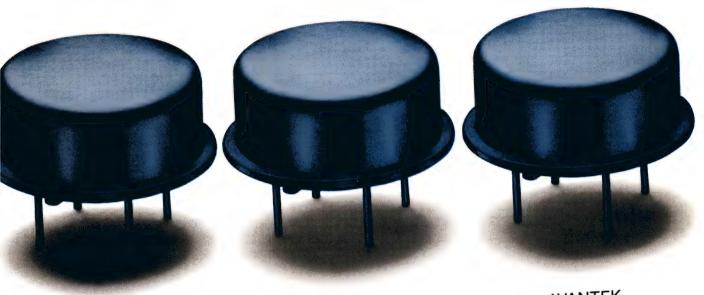


Fig 1—The programs in the listings simulate the action of this XOR-feedback shift register of length n, which can generate a pseudorandom pattern that repeats every 2^{n-1} bits.

and to generate simulated random inputs. The program is available directly from the author for a nominal fee. Send requests to the author at Qualcomm, 10555 Sorrento Valley Rd, San Diego, CA 92121, or phone (619) 587-1121, ext 472.

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Three methods protect $\mu PI/O$ lines

Richard J Valentine Motorola, Phoenix, AZ

The three circuits in Fig 1 protect a μP 's I/O lines against transients. These circuits have proved their worth in numerous, severe automotive applications. All three employ a 100-kHz low-pass filter formed by a 0.01- μF capacitor and a 5.1-k Ω resistor.

In Fig 1a, a 5.1V Zener diode clamps positive-going transients, and a Schottky rectifier clamps negative-going transients. The Schottky rectifier has problems at both ends of the temperature scale. At 125°C (257°F), its leakage current may reach 50 μA when the input line is at 5V. This leakage is not a big deal unless the input resistor has a value of 100 k Ω or more.

More troubling, at temperatures below -40° C (-40° F), the Schottky rectifier's forward voltage rises to about 0.47V, which is perilously close to the -0.50V max spec most HCMOS-type μ P's inputs can tolerate.

In the second circuit, Fig 1b, Schottky rectifiers clamp both positive- and negative-going voltage transients.

The third circuit, **Fig 1c**, uses two regular silicon rectifiers. One rectifier is connected in series with the input line, thereby isolating the μ P's inputs from negative-going voltage spikes. The other rectifier is in series with a 5.1V Zener, which clamps positive-going transients. Because the μ P's input-line series rectifier subtracts 0.7V from signals seen by the μ P, you must insert the other rectifier in the Zener's circuit to bring

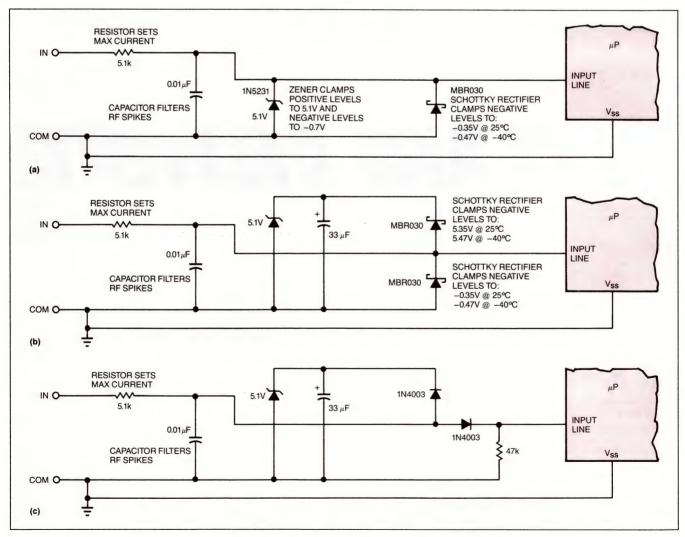


Fig 1—These three circuits protect a μ P's input lines from destructive transients.

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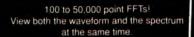
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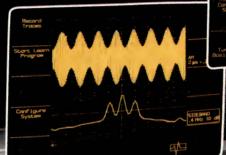
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DESIGN IDEAS

the clamping voltage up to 5.7V. This addition ensures that the μP will see 5V max and not 4.3V max.

Your pc-board or thick-film design layout can also affect the μP 's reliability in the face of overvoltage transients. Locate the clamping networks close to both the input-socket pins and to ground. The μP 's own ground traces should not be in the path of any voltage-

clamping networks. You may also find that placing a metal shield around the μP 's pc-board area protects the μP against radio-frequency interference and electrostatic discharge.

To Vote For This Design, Circle No 753

Optoisolators protect solid-state relay

Brady Barnes
Inter-Tel, Chandler, AZ

The circuit in Fig 1 protects a solid-state relay from overloads. The circuit limits current, automatically disconnects the load after detecting a short circuit, and develops a fault-condition output signal.

In normal operation, the controlling μP sets the flip-flop, IC₁, which turns on transistor Q₁. When Q₁ turns on, current flows through the solid-state relay's input, thus activating the relay.

If an overcurrent or fault condition occurs, the excessive load current flowing through the relay develops enough potential across sense resistor R_5 to turn on one of the optoisolators, IC_{4A} or IC_{4B} . The optoisolator's output transistor diverts current around the solid-state

relay's input, which limits the current the relay's output can pass.

If the overload is severe enough, the optoisolator pulls the input of the Schmitt trigger above its threshold, thus clearing the flip-flop and turning off the solid-state relay. R_2 has two functions: It keeps the input of the Schmitt trigger below 5V max to prevent latchup, and it forms an RC filter in conjuction with C_1 . The RC filter prevents spurious triggering of the Schmitt trigger.

You can use the output of the flip-flop to signal overload conditions to the controlling μP .

To Vote For This Design, Circle No 754

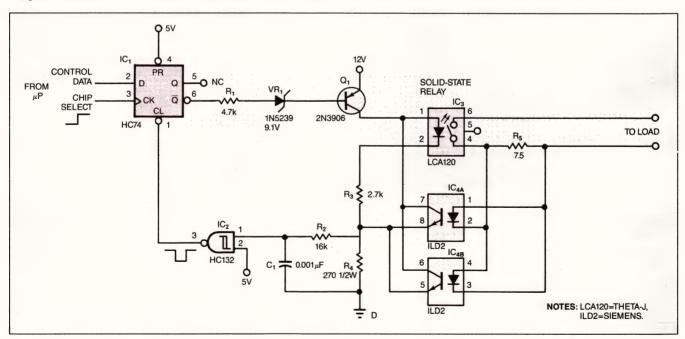


Fig 1—When optoisolator IC_4 detects excessive current in sense resistor R_5 in the solid-state resistor's load path, the optoisolator diverts current around the solid-state relay's control input. If the overload is severe enough, the optoisolators trigger the Schmitt trigger, which clears the flip-flop and turns off the solid-state relay.

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Hex error messages suit assemblers

Charles H Small EDN, Newton, MA

When you're developing a program in assembly language and have reached that frustrating, shaky stage where various unknown problems cause your program to die repeatedly, error messages often prove handy during post mortems. Cooking up error messages is easy for software engineers who enjoy the luxury of high-level languages because these languages have built-in functions for outputting ASCII strings. Assembly-language programmers must fashion their own tools.

A primitive, assembler-compatible scheme capitalizes on the possibility of spelling words with hex numbers. For example, $DEAD_{HEX}$ is, after all, a condition as well as a hex number. If you need more than one error message, you can use $DED1_{HEX}$, $DED2_{HEX}$, $DED3_{HEX}$... $DED9_{HEX}$.

If you're willing to squint a bit and read some numerals as letters, you can also enter "died" as $\rm D1ED_{HEX}$ and use $\rm B00B_{HEX}$ to signal that your program has done something stupid.

One way to employ these assembler-compatible error messages is to fill unused portions of memory with NOPs. At the very end of a field of NOPs, insert two commands: one to write an error message—say,

DEAD $_{\rm HEX}$ —to a handy memory location, I/O port, or μP register; and another to jump to a reset routine. This trick lets your program recover gracefully from an erroneous jump to the wrong memory area and leaves a record of where the program went wrong. And you won't have to bother with laboriously inserting ASCII strings into your assembler code; your assembler will happily digest these error messages as if they were just hex numbers.

During debugging, you needn't feel envious of high-level programmers and their high-level-syntax debuggers—even the simplest debug monitor can get your error messages from a memory location or μP register and display them in readable form. Statistically speaking, this scheme is fairly foolproof; only a few chances in 64k exist that your crashing program will overwrite your error-message location with a readable error message. Most of the time, you'll probably see the usual gibberish.

You can also employ a more scattershot approach by appending a small NOP field followed by the errormessage-writing and jump-to-reset instructions to every subroutine after its normal exit instruction. This trick may gently shortstop an erratically careening program before it crashes. (This hint courtesy Richard Valentine, Motorola, Phoenix, AZ.)

FEEDBACK AND AMPLIFICATION

Routine obviates self-modifying code

Noor Singh Khalsa's Design Idea, "Alterable code enhances instructions" (EDN, May 12, 1988, pg 210), reminded us of an application requiring indexed bit access in the 8031 single-chip μ P. (Ed Note: Copy editing altered the original title of Mr Khalsa's Design Idea, which read "Self-modifying code enhances instructions.") Our approach is somewhat different from Mr Khalsa's and requires no special hardware or self-modifying programs.

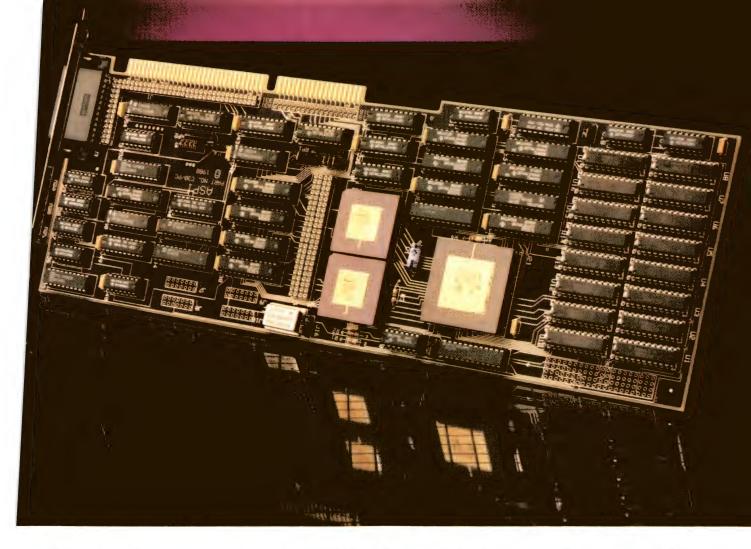
The two routines in **Listing 1** set and clear, respectively, a bit whose composite address you put in the accumulator before calling the routines. The subroutine BREAK splits this composite address into two parts: an address in the BYTE address space and the number of the individual bit to be cleared or set. BREAK uses this formula:

Byte_ad = Bit_ad DIV 8 + 20H; {Returned in R1} Bwib = Bit_ad MOD 8; {Returned in R0}.

Then BREAK creates a bit mask. Depending on whether you wish to set or clear the bit, the routine makes a mask by shifting a single 1 into the proper position in a byte of zeros or a single 0 in a byte of ones. A byte-wide OR with the first mask will set the bit; a byte-wide AND with the second mask will clear the bit.

This approach does not require overlapping the single-chip $\mu P's$ RAM and ROM address spaces and does not modify executable instructions.

Gary Lynch, R&D Staff Engineer IMO Industries Inc 3750 E Market St York, PA 17402



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ISSUE WINNER

The winning Design Idea for the June 8, 1989, issue is entitled "Power isolators are bidirectional," submitted by John LaBelle of Logical Control Engineering (Long Beach, CA).

Your vote determines this issue's winner. All designs published win \$100 cash. All issue winners receive an additional \$100 and become eligible for the annual \$1500 Grand Prize. Vote now, by circling the appropriate number on the reader inquiry card.

FEEDBACK AND AMPLIFICATION

LISTING 1 8031 INDEXED-BIT ROUTINES

```
Indexed bit set operation
    (ACC holds bit address upon entry)
SET BIT A:
              BREAK
                              ; Break into byte and BwiB address
        MOV
                A,#01H
                              ; Set up OR mask
        CALL
                MASK
        ORI
                A, @R1
                              ; Set appropriate bit
        MOV
                @R1.A
    Indexed bit clear operation
    (ACC holds bit address upon entry)
CLR_BIT_A:
ACALL
                              ; Break into byte & Bw/iB addresses
                BREAK
        MOV
                A, #NOT(01H); Set up AND mask
        CALL
                MASK
                A. ORI
                              ; Clear appropriate bit
        ANI
        MOV
BREAK: MOV
                B,#8
        DIV
                RO,B
        MOV
        ADD
                A. #20H
MASK:
        CJNE
                R0, #0, LOOPM
        RET
LOOPM:
        DJNZ
                RO, LOOPM
```

Updated program speeds calculations

Since the publication of my Design Idea, "Program speeds best-fit 1% resistor calculations" (*EDN*, July 7, 1985, pg 308), I have come up with a greatly improved version of the program. I'd be happy to send a copy of the new and improved version to anyone who will send me a self-addressed stamped envelope.

Andrew K Dart Andy's Bureau of Standards

Box 380508

Duncanville, TX 75138

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Editors regret figure mixup

Sharp-eyed readers have probably already spotted the mixup in the Design Ideas section of the June 22, 1989, issue of *EDN*. The **Fig 1**s accompanying "Triacs preregulate HV supply" by Héctor Gellon on page 236 and "True-rms AGC provides constant power" by Mark Murphy on page 238 were inadvertently switched. Please note that the captions are correctly placed.

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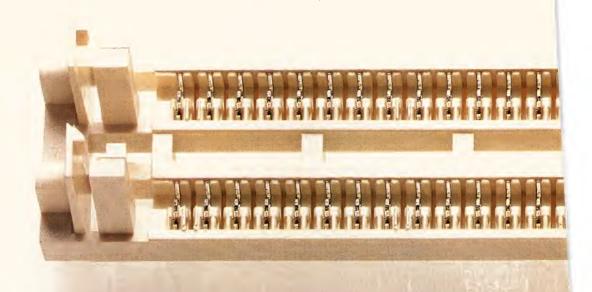
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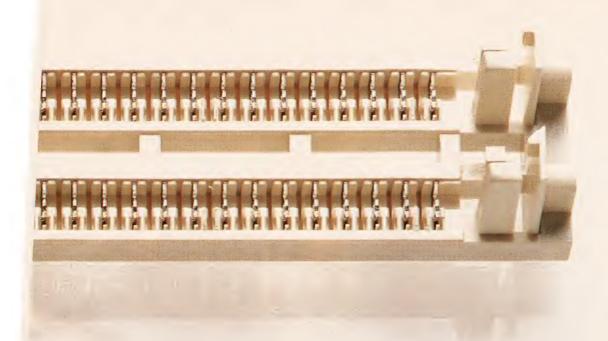
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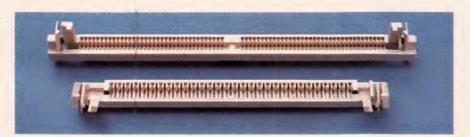
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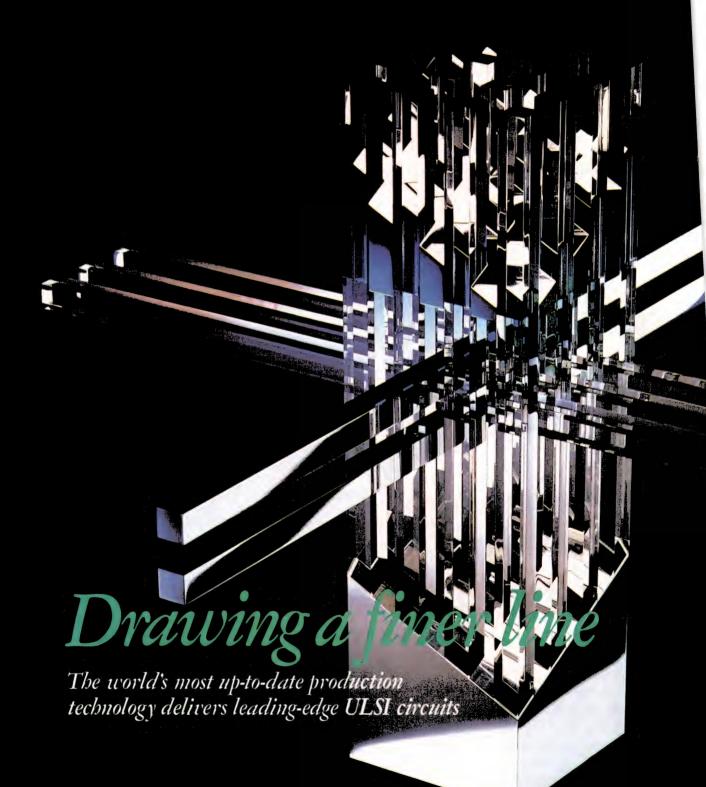
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Circle No 360

EMULATOR CABLES

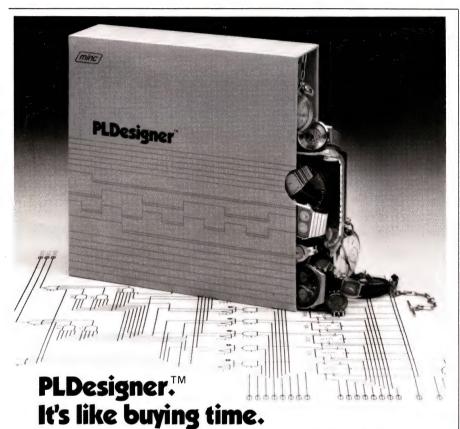
- Replace DIP/PLCC converters and DIP extension cables
- Connect ICE without removing adjacent pc boards

The EXT40/44A-2X transmissionline extension cables convert from 40-pin DIP to 44-pin PLCC (plastic leaded chip carrier) termination. The units are designed to connect between the pod of an in-circuit

emulator for the 8051 microcomputer and the target system's processor socket. Each cable replaces two parts—a DIP extension cable and a DIP/PLCC converter-and has a profile lower than that of the two parts. The low profile permits the plug-in units to function in many situations that would otherwise require removal of an adjacent pc board. To provide low crosstalk and controlled impedance, each signal wire is paired with a ground wire. In 6-, 9-, and 12-in. lengths, \$220, \$224.50, and \$229, respectively.

EDI Corp. Box 366, Patterson. CA 95363. Phone (209) 892-3270.

Circle No 361



Cut weeks from your complex PLD logic designs. PLDesigner design synthesis system combines powerful design entry with automatic design partitioning and device selection to automate time consuming design steps.

With PLDesigner, you enter and simulate the design before device implementation. PLDesigner automatically partitions the design and presents device solutions from a 2500 device library that includes advanced architecture devices. No more manual partitioning, data-book searches or trial-anderror design.

Enter designs using a high-level language, waveforms, or schematic entry to speed design creation. Combine several designs into a system to reduce IC count, cost and PC-board space.

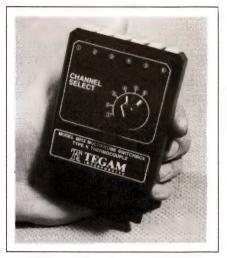
The process is executed automatically...including pin assignments, documentation, test vectors, and programmer setup to get the job done faster.

PLDesigner runs on the PC and is the only PLD solution to be fully integrated into the Mentor Graphics, Cadnetix, and Intergraph environments.

See what it's like to buy time and get your designs to market faster. Call for a FREE demo package.

Minc Incorporated 1575 York Road, Colorado Springs, CO 80918 719-590-1155





SWITCH SERIES

- Allows connection of six TC probes to one thermometer
- Available for type J, K, and T probes

The 8000 series of multiprobe switch boxes allows you to connect six thermocouple probes to a single thermometer, and to select among the probes, using a rotary switch. The switch boxes, which are available for type J, K, and T probes, work with standard extension cables. \$89.

Tegam Inc, 7230 N Ridge Rd, Madison, OH 44057. Phone (216) 428-7505, FAX 216-428-1068.

Circle No 362



MIXED-SIGNAL TESTER

- Verifies analog/digital ASIC designs
- Lets you integrate IEEE-488 instruments you select

The Logic Master XL Mixed-Signal Verification System extends the vendor's digital ASIC-verifiers to

On universal standby. With double overcharge protection.

VARTA – worldwide leader in NC Button Cell technology again demonstrates their ability to innovate – has now developed a new generation of rechargeable NiCd Button Cells capable of accepting high rates of trickle charge currents. Even when fully charged, these cells can still be overcharged at currents of up to 0.2 CA (2 x 110) without risk of failure and are therefore ideal for continuous charging in standby applications. The new VARTA V...R cells you can rely on.

With up to 12% higher capacities than the proven DK cells and with a fast recharge capability of 7-hours in addition to the normal 14-hours. When trickle charging, the cells can be used with currents of between 0.01 CA (0.1×110) and 0.05 CA (0.5 x I10). Why not enhance your product features with a high reliability standby power source.

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allow characterization and design verification of analog/digital devices with as many as 176 digital I/O pins. The heart of the analog portion of the 80386-based system is a wideband, low-noise switching matrix that resides on the IEEE-488 bus. You can add IEEE-488 instruments of your own choosing to the system, and the software will allow you to write procedures to control them. You can then integrate these procedures into larger device-test programs. The system's digital I/O channels operate to 100 MHz with a ±1-nsec timing skew. From \$120,000. Upgrades to existing Logic Master XL systems, from \$60,000. Delivery, fourth quarter 1989.

Integrated Measurement Systems Inc, 9525 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-7117. FAX 503-644-6969.

Circle No 363



SPECTRUM ANALYZER

- Covers 10 kHz to 21 GHz
- Offers −103-dBc/Hz sideband noise at 30-kHz offset

The 492PGM portable microwave spectrum analyzer covers a frequency range of 10 kHz to 21 GHz. It has an 80-dB dynamic range and can measure frequency with 0.001% accuracy. At an offset of 30 kHz from a carrier, sideband noise is –103 dB below the carrier level. Residual frequency modulation is 12 Hz p-p. The unit automates the measurement of filter bandwidth

and includes an automatic normalization feature to eliminate calculations when determining carrier-to-noise ratios. It also automatically converts signal levels to decibels with respect to several reference levels and can directly drive a graphics plotter. \$19,900. Delivery, six weeks ARO.

Tektronix Inc, Box 500, Beaverton, OR 97077. Phone (800) 835-7732; in OR, (503) 235-7315.

Circle No 364

A/D I/O CARD

- Includes ADC, DAC, digital I/O, and timer/counter
- Offers eight differential or 16 single-ended analog inputs

The R718 is a multifunction analog/digital data-acquisition card for the IBM PC bus. A 12-bit ADC samples at 100k samples/sec and can accept data from eight differential or 16



TEST & MEASUREMENT INSTRUMENTS

single-ended channels. The unit, which implements direct-memory access, also includes a DAC, an ADC, a timer/counter, and digital input and output ports. A companion utility software disk contains high-level command routines, sample programs, and routines for linearizing transducer outputs. \$1495.

Rapid Systems Inc, 433 N 34th St., Seattle, WA 98103, Phone (206) 547-8311. FAX 206-548-0322.

Circle No 365

550-MHz COUNTER

- Operates to 100 MHz in direct mode
- Offers 50-mV-rms sensitivity at 550 MHz

The Model 1804 makes direct 8-digit frequency measurements from 5 Hz to 100 MHz with 1-Hz resolution and, with its internal prescaler,



measures from 10 to 550 MHz with 10-Hz resolution. Resolution stated is obtained with a 0.1-sec gate interval in direct mode and a 1-sec gate interval in prescaled mode. The direct input has an impedance of 1 $M\Omega$ shunted by 40 pF; the prescale input has an impedance of 50Ω . Sinewave sensitivity in prescaled mode is 50 mV rms throughout the useful frequency range. A 100-kHz lowpass filter is switch selectable. \$295.

B&K Precision, 6470 W Cortland Ave, Chicago, IL 60635. Phone (312) 889-9087.

Circle No 366







- 100% IBM-AT Compatible STD Bus **Industrial Computer**
- Fast 10, 12, 16 or 20 MHz 80286 CPU
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CIRCLE NO 98

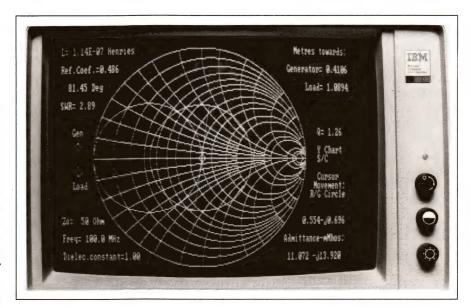
NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

RF DESIGN TOOL

- Creates Smith charts to aid in analysis of transmission lines
- Allows for line losses and provides a reference mode

Z-Match is an RF-design program that runs on IBM PCs and compatibles, and handles the calculation and conversion of impedance and admittance, parallel and series network equivalents, wavelengths, distances, characteristic impedance (Z₀), dielectric constants, reflection coefficients, standing-wave ratios, and Q values. The program creates a Smith chart based on two sets of circles, one of which represents the resistive component and the other the reactive component. The circular properties of the chart let you make calculations of impedances, admittances, SWRs, and Q values, by simple geometric constructs, and read off actual values at the cursor



position. You can directly implement the solutions that you find with the aid of Z-Match with transmission-line transformer and stubmatching methods, using coaxial cables, microstrip, stripline, and

waveguides. £130.

Number One Systems Ltd, Harding Way, Somersham Rd, St Ives, Huntingdon, PE17 4WR, UK. Phone 0480 61778.

Circle No 351

80386 CROSS-DEBUGGER

- Lets you debug 32-bit protectedmode software
- Works with a monitor resident in the target system's ROM

Soft-Scope III/386 is a source-level cross-debugger that runs on an IBM PC/AT or compatible machine and lets you debug 32-bit protectedmode software for an 80386- or 80486-based target system. The debugger communicates with Intel's iM III monitor, resident on the target system, over a serial communications link. Soft-Scope III and iM III can work with 80386, 80386SX, 80376, and 80486 processors. The debugger provides advanced symbolic capabilities and allows you to view any user-declared symbol (including structures, multidimensional arrays, unions, and bit fields) by means of a symbolic, formatted display. The debugger also provides a C-like macro facility and the ability to evaluate complex symbolic expressions. The program reports hardware protection traps, such as stack overflow and segment overrun, at the source-code level, and allows you to view protected-mode structures such as global and local descriptor tables. The debugger is compatible with a variety of programming languages, such as Intel's ASM386, PLM386, and C386, as well as Metaware's High C-386 and PharLap's 386/ASM. \$1500.

Concurrent Sciences Inc, Box 9666, Moscow, ID 83843. Phone (208) 882-0445. FAX 208-882-9774.

Circle No 352

AUTOROUTER

- Can handle six signal layers as well as power and ground layers
- Can handle as many as 3500 components and 10,000 pads

Traxstar is a grid-based, costed maze autorouter with full rip-up and reroute capability. The pro-

gram can handle six signal layers in addition to separate power and ground layers. Depending on the amount of available memory, your design can have as many as 3500 components, 10,000 pads, and 12,000 connections on a board as large as 20×32 in. The program performs several passes: A pattern router recognizes specific vertical and horizontal patterns for fast routing; a maze-expansion router optimizes costing for both speed and very high levels of completion; a rip-up and reroute pass routes any remaining connections and, in case of collision, rips up and reroutes the previously routed tracks and vias; and a rip-up and smooth pass rips up and reroutes connections with the goal of reducing track length and via count. The costing structure is user definable and allows you to assign different cost factors for each pass. The program can work with either through-hole or surfacemount technologies and incorporates a separate plot/print utility. To run the program, you'll need an IBM PC, PS/2, or compatible that runs under PC-DOS 2.0 or a later version and that has 640k bytes of RAM, a color-graphics adapter, and two floppy-disk drives (a hard-disk drive is preferable). \$995.

Protel Technology Inc, 50 Airport Pkwy, San Jose, CA 95110. Phone (408) 437-7771. FAX 408-437-4913.

Circle No 353

ADA TOOL SET

- Includes a language-sensitive editor
- Provides interactive cross-referencing

TeleArcs is an integrated set of tools for the detailed-design, development, and test stages of Ada software created with the aid of the

TeleGen2 Ada compilation system. Written entirely in Ada, the tool set includes an EMACS-like Adasensitive editor; a graphical systemdisplay and -browsing facility; and facilities for arbitrating changes to shared code. The editor processes source-code and provides syntax checking, interactive cross-referencing, error feedback, "pretty print" formatting, and hierarchical text presentation. A key-binding feature lets you assign editing commands and other command strings to individual keys. The browsing feature lets you view program units, import relationships, dependencies, and other important data. Configuration and baselining features allow you to check out and check in shared compilation units. and thus act as a librarian to arbitrate changes to shared code. Other features, such as macros, command history, window management, and

on-line help, all use the inherent da tabase facilities of the TeleGen? Ada Library to accumulate extensive information about the application you're developing and make it easier for members of a programming team to maintain accuracy and consistency throughout all phases for the development cycle. From \$4500 for Sun-3 or VAX/VMS computers.

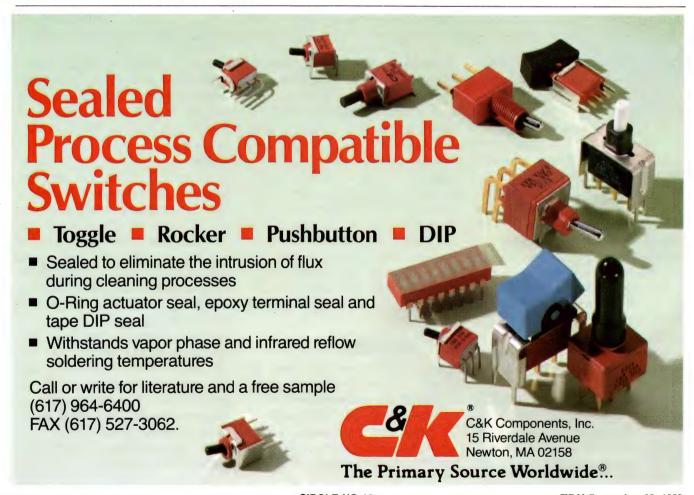
TeleSoft AB, 5959 Cornerstone Ct W, San Diego, CA 92121. Phone (619) 457-2700. TLX 855300. FAX 619-452-1334.

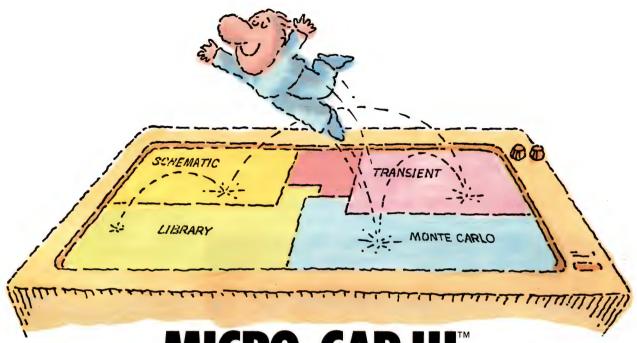
Circle No 354

ADA FOR PCs

- Validated under ACVC 1.10
- Incorporates a complete Chapter 13 implementation

AdaVantage version 3.0 provides a complete Ada development system for IBM PCs, PS/2s, and compa-



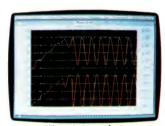


MICRO-CAP III. THIRD-GENERATION INTERACTIVE CIRCUIT ANALYSIS. MORE POWER. MORE SPEED. LESS WORK.

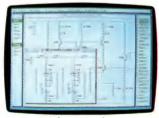
MICRO-CAP III,™ the third generation of the top selling IBM® PC-based interactive CAE tool, adds even more accuracy, speed, and simplicity to circuit design and simulation.

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Transient analysis



Schematic editor



Monte Carlo analysis

Modeling power leaps upward as well, to Gummel-Poon BJT and Level 3 MOS—supported, of course, by a built-in Parameter Estimation Program and extended standard parts library.

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Naturally, you'll want to call or write for a free brochure and demo disk.



1021 S. Wolfe Road, Sunnyvale, CA 94086 (408) 738-4387

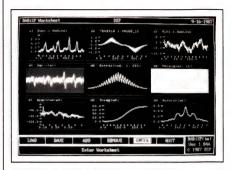
MICRO-CAP III is a registered trademark of Spectrum Software. Hercules is a registered trademark of Hercules Computer Technology. IBM is a registered trademark of International Business Machines, Inc. tibles. The package includes an Ada compiler, a source-level debugger, an Ada Developer Interface, a DOS environment library, and a utility library. This new version has been validated under ACVC 1.10, and incorporates a complete Chapter 13 implementation, including representation specifications for variant

or discriminant records, task-interrupt entries, and length clauses that include size specifications and access-type storage collections. This version allows you to compile generic specifications and bodies separately to improve the handling of complex generics; provides improved interface support for Intel

assembly-language programs and enhanced runtime compatibility for Microsoft C programs; and allows the use of unsigned integers. To use the package, you'll need 640k bytes of RAM and a hard disk. Professional Developer Kit, \$1780; Developer Kit, \$1095.

Meridian Software Systems Inc, 23141 Verdugo Dr, Suite 105, Laguna Hills, CA 92653. Phone (714) 380-9800.

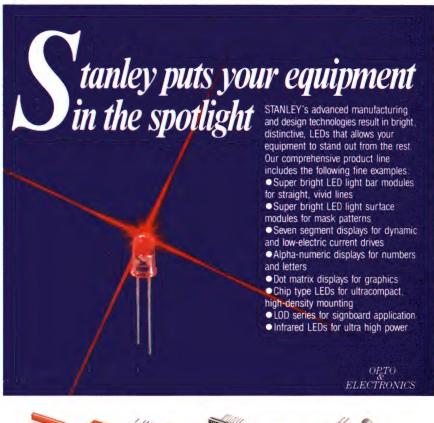
Circle No 355

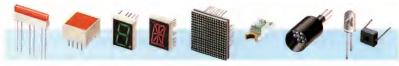


DSP ANALYSIS TOOL

- Acts like a spreadsheet for waveforms and graphs
- Can display as many as 64 separate windows

Dadisp is a graphical, post-acquisition program for data analysis and digital signal processing. You can display as many as 64 separate windows, each representing a waveform previously imported into Dadisp; if you enter a formula into the window, the display shows the result of processing the waveform by that formula. If your waveform is too large for system memory, the program automatically pages the waveform to and from your disk during most calculations. You can apply more than 200 analysis routines to any waveform; the routines include signal arithmetic, signal calculus, waveform generation, Fourier analysis, frequency-domain analysis, correlations, and statistical routines. The program can also handle complex numbers and engineering-unit conversions. The new version of the program, which runs on IBM PCs, PS/2s, and compa-





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CIRCLE NO 18

CAE & SOFTWARE

tibles, can now control laboratory instruments via an IEEE-488 bus. and it lets you build menus that automate the execution of frequently used but complex command sequences. PC version, \$1695; workstation versions, \$6900 to \$7500, depending on the host configuration.

DSP Development Corp, 1 Kendall Sq, Cambridge, MA 02139. Phone (617) 577-1133. FAX 617-494-1394.

Circle No 356

BOARD-DESIGN TOOL

- Contains new libraries of parts and simulation models
- Creates custom drivers for 93 EGA and VGA compatibles

OrCAD/SDT III version 3.21 is a schematic-capture tool that's been enhanced by many new features. New libraries of Altera, Intel, and generic PLDs raise the total number of parts in the vendor's libraries to more than 6200. The tool can also use other libraries from third-party vendors. There is a library of simulation primitives for use with the vendor's OrCAD/VST 1.20 logic simulator. A new utility can create custom drivers for as many as 93 different EGA- and VGA-compatible monitors. In addition, the package provides three new videodisplay drivers for monitors that have 1024×788 -pixel resolution. The field-stuffing utility, which puts information from a text file onto the schematic, now includes a new feature that generates an activity report. An enhancement to the graphical library editor retains the identification of the source library from which you originally obtained a given part. \$495. Registered users of previous versions that are still under warranty can upgrade at no charge.

OrCAD Systems Corp, 1049 SW Baseline St, Suite 500, Hillsboro, OR 97123. Phone (503) 640-9488.

Circle No 357

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- Program several boards in one pass
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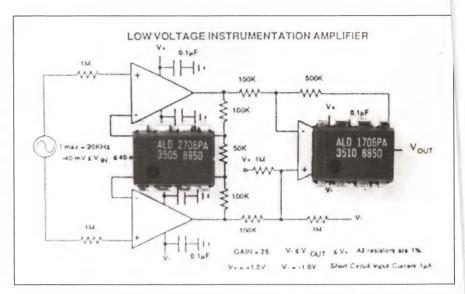
NEW PRODUCTS

INTEGRATED CIRCUITS

DUAL OP AMP

- Needs only 20 µA per channel
- Features rail-to-rail operation

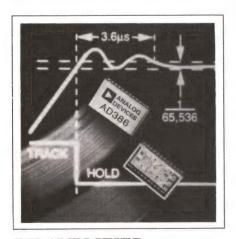
Characterized for a 5V single supply or a ± 2.5 V dual supply, the ALD-2706 dual op amp is suitable for use with supply voltages from 2 to 12V and ± 1 to $\pm 6V$. With a 5V supply, the typical operating current is only 20 µA per amplifier. Each amplifier can operate with rail-to-rail input and output voltages. This feature provides flexibility in input signal bias levels, which is important for low-voltage applications and critical for supply voltages at or below 2V. A typical amplifier can process a 0.9V analog signal with just a 1V supply. Each output stage can drive a 50-pF and 20 $k\Omega$ load. The op amp also features an open-loop gain of 100V/mV, a



gain-bandwidth product of 300 kHz, and a slew rate of $0.17 \text{V}/\mu\text{sec}$. Three offset-voltage grades of 2, 5, and 10 mV are available. In a plastic DIP, \$3.84 (100).

Advanced Linear Devices, 1180F Miraloma Way, Sunnyvale, CA 94086. Phone (408) 720-8737. FAX 408-720-8297.

Circle No 375



T/H AMPLIFIER

- Features 16-bit accuracy
- Has internal hold capacitor

The AD386 is a true 16-bit track and hold (T/H) amplifier that features 0.00076% linearity over the extended industrial-temperature range of -40 to +85°C. The AD386, which contains an internal hold capacitor, acquires signals within its 20V span in 3.6 µsec typ. Other important specs include an aperture uncertainty (jitter) of only 40 psec and a 2-MHz bandwidth.

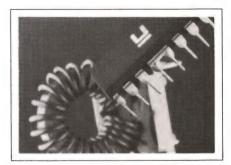
Unlike many T/H amplifiers, the AD386 contains an uncommitted, unity-gain differential amplifier. This amplifier reduces commonmode errors caused by ground-potential differences; it also provides a convenient way to reverse the polarity of the analog signal. 24-pin, double-width ceramic DIP, from \$79.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (508) 658-9400.

Circle No 376

MAG-AMP CONTROLLER

- Provides a 100-mA reset current
- Controls current from 2 to 20A
 The UC3838A contains circuitry to
 generate and amplify an analog error signal. In addition, a high-voltage current source provides a reset
 current as high as 100 mA to enable
 a magnetic amplifier to regulate and
 control the output of a 2 to 20A
 power supply. By controlling the
 reset current to a magnetic ampli-



fier, the UC3838A defines the amount of volt-seconds the amplifier blocks before switching to the conducting state. Using the UC3838A, only the magnetic amplifier coil, three diodes, and an output LC filter are needed to implement a complete closed-loop regulator. The UC3838A includes a precision 2.5V reference, two uncommitted high-gain op amps, and a high-gain pnp-equivalent current source. 16pin DIP, from \$1.90 (1000).

Unitrode Integrated Circuits Corp, 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410.

Circle No 377

SUPER FAST SRANS, PRODUCTION PROVEN.

When you work at the leading edge of technology, you need components that are production proven — not still in development.

At Micron Technology, we've applied the same state-of-the-art design and process technology used for our high quality DRAMs in development of our Fast Static RAMs. The result — an incredible 25ns 256K and 15ns 64K and 16K, plus a full line of other super fast parts. And we're not just sampling product, we've been shipping production volumes for over a year.

A wide variety of packages, densities and organizations are offered to meet all your application needs. And like all Micron memory products, our

Fast SRAMs are backed by the type of strong sales, customer service and technical support that keeps you on the leading edge.

So get the Super Fast SRAMs you need now by calling us at 1-208-386-3900.

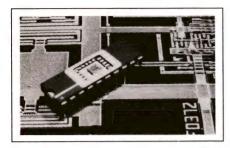
Micron. Working to improve your memory.

Available Now! 256K 25ns 64K 15ns/16K 15ns

Part #	Organization	Speed*	Packages
MT5C2561	256K X 1	25ns	PDIP, CDIP, SOJ, LCC
MT5C2564	64K X 4	25ns	PDIP, CDIP, SOJ, LCC
MT5C2565	64K X 4 OE	25ns	PDIP, CDIP, SOJ, LCC
MT5C2568	32K X 8	25ns PDIP, CDIP, SOJ, LCC	
MT5C6401	64K X 1	15ns	PDIP, CDIP, SOJ
MT5C6404	16K X 4	15ns	PDIP, CDIP, SOJ
MT5C6405	16K X 4 OE	15ns	PDIP, CDIP, SOJ
MT5C6406/7	16K X 4 S. I/O	15ns	PDIP, CDIP, SOJ
MT5C6408	8K X 8	15ns	PDIP, CDIP, SOJ, LCC
MT5C1601	16K X 1	15ns	PDIP, CDIP, SOJ
MT5C1604	4K X 4	15ns	PDIP, CDIP, SOJ
MT5C1605	4K X 4 $\overline{\text{OE}}$	15ns	PDIP, CDIP, SOJ
MT5C1606/7	4K X 4 S.I/O	15ns	PDIP, CDIP, SOJ
MT5C1608	2K X 8	15ns	PDIP, CDIP, SOI



2805 E. Columbia Road, Boise, Idaho 83706 208-386-3900



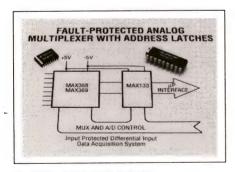
FERROELECTRIC IC

- Features 1-year data retention
- Compatible with 74HCT logic

Compatible with industry-standard 74HCT logic, the K74CF372 is an 8-bit, flip-flop logic IC that saves its states in nonvolatile memory. The IC stores data provided to its inputs on every positive clock transition and recalls stored data to its outputs when the recall signal is given after repowering the system. The K74CF372 features data retention of more than 1 year between uses after 10¹¹ data changes. It also features a 300-kHz access rate for fast parameter storage. Fabricated in low-power CMOS, the device needs <1 mA of current in the active state. 20-pin ceramic DIP, \$8.50 (100).

Krysalis Corp, 1135 Kern Ave, Sunnyvale, CA 94086. Phone (408) 749-7390. FAX 408-749-7390.

Circle No 378



MULTIPLEXERS

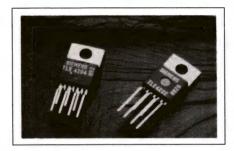
- 4- and 8-channel versions
- Include fault protection

The Max368 and Max369 fault-protected analog multiplexers come with on-chip data latches. The latches relieve the μP from supplying constant addresses to the logic inputs. The Max368 has eight sin-

gle-ended inputs: the Max369 has four differential inputs. Protecting the multiplexers, as well as the source and output circuitry, is a feature that limits leakage current to a few nanoamps if power to the multiplexers is removed while the input voltage is still applied. All channelselection and control inputs are compatible with both TTL and CMOS logic levels. The multiplexers work with either a single supply of 9 to 22V or dual supplies of ± 4.5 ±18V. Three temperature grades are available. 16-pin DIP, from \$6.36 (1000).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 379



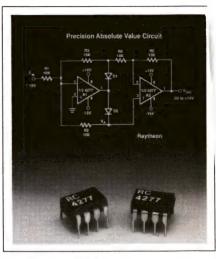
MOTOR DRIVERS

- Contain 42V-rated bridge
- Current ratings to 4A

Designed to drive small motors in industrial and automotive applications, the TLE 4200 series of bridge-circuit motor drivers is rated at 42V. The ICs include protection for short circuits and overtemperature conditions. Current ratings are 2, 3, and 4A, respectively, for the TLE 4202B, TLE 4204, and TLE 4203. Using logic-level inputs, the drivers can control the rotation, acceleration, and braking of dc motors. The devices are rated for operation over the -40 to +125°C temperature range. \$2.38 to \$3.65 (10,000).

Siemens Components Inc, Integrated Circuits Div, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4598.

Circle No 380



DUAL OP AMP

- Has low input-offset voltage
- Has high open-loop gain

Available in an 8-pin DIP, the RC4277 bipolar dual op amp features high packing density and precision performance. Input offset voltage is only 30 μV max with V_{os} drift of 0.5 µV/°C max. Open-loop gain is a minimum of 2,000,000 into a 2000-k Ω load, and input bias current is a maximum of ±3 nA. Maximum power consumption for both channels is only 100 mW. Other specs include a CMRR and a PSRR of 120 dB min. The RC4277 is designed to replace other amplifiers such as the OP200, OP207, LT1001, LT1013, OP07 and OP77. From \$2.95 (100).

Raytheon Co, Semiconductor Div, 350 Ellis St, Mountain View, CA 94043. Phone (415) 968-9211.

Circle No 381

CMOS SEMICUSTOM ICs

- Gate arrays
- Standard cells

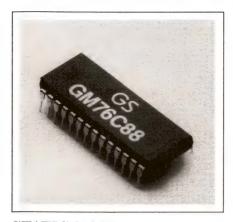
The MSM7U000 family of channeled gate arrays offers clock rates to 80 MHz and propagation delays of 460 psec. The arrays feature gate counts from 1632 to 30,384 and I/O pins from 60 to 252. All of the arrays have an output drive capability of 48 mA, which permits high-speed operation under heavy loads. The MSM91U000 series of standard-cell

INTEGRATED CIRCUITS

levices features a library of 160 small-scale and 88 medium-scale olocks, 39 hardware macros, and most of the 82Cxx-product macros. Also available are static RAMs to 32k bits and ROMs to 128k bits. From \$2 (10,000).

Oki Semiconductor, 785 N Mary Ave, Sunnyvale, CA 94086. Phone (408) 720-1900. FAX 408-720-1918.

Circle No 382



STATIC RAM

- Organized as $8k \times 8$ bits
- Available in three speed ratings Organized as 8192 words×8 bits, the GM76C88 65,536-bit CMOS static RAM operates from a 5V supply and features both low-power and high-speed operation. Maximum operating current is 80 mA, and speed selections of 85, 100, and 120 nsec are available. In 28-pin plastic DIPs, \$3 to \$4 (100).

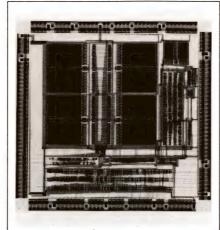
Goldstar Technology Inc, 1130 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 737-8575.

Circle No 383

CACHE CONTROLLER

- Supports Intel 80386 CPU
- Works at 20-, 25-, and 33-MHz The MDS-C395e 32-bit cache co

The MDS-C395e 32-bit cache controller supports 32k, 64k, 128k, and 256k bytes of cache memory. Designed for use with Intel's 80386 CPU, the C395e works with 20-, 25-, and 33-MHz systems. The controller supports 4-way, set-associative configurations as well as direct-



mapped and 2-way, set-associative configurations. The C395e offers copyback, write-through, and posted writes for maintaining mainmemory coherency with the cache. The copyback scheme frees up system bus bandwidth for other tasks such as DMA. To interface with the 80386, the C395e requires only four 8-bit data transceivers for external logic. 164-lead flatpack, \$174 (100).

Matra Design Semiconductor, 2895 Northwestern Pkwy, Santa Clara, CA 95051. Phone (408) 986-9000. FAX 408-748-1038.

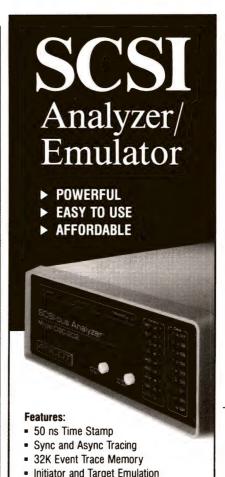
Circle No 384

1M-BIT ROMs

- Have speeds of 150 and 200 nsec
- Have user-definable control pins Featuring response times of 150 and 200 nsec, the 28-pin 631000 and 32-pin 631001 ROMs have 1M-bit storage capacities. The devices, which operate from a 5V supply, provide flexible design options via four user-definable control pins. Using the 631000 or 631001, system designers can link as many as 16 of the ROMs on a single data bus. The ICs are available in temperature ranges for commercial, industrial, and military applications. From \$5.50 (10,000).

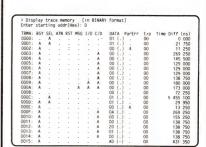
Gould Inc, Semiconductor Div, 2300 Buckskin Rd, Pocatello, ID 83201. Phone (208) 234-6851.

Circle No 385



> Display trace memory [in structured format]
Enter starting add(field): 0
0001: Abitation /80
0003: Select w.1Ah /C0
0006: Message-0ut/CO(Identify)
0007: Command /12(Inquiry) 00 00 00 30 40 4f 4f 45 52 20 20
0000: Dist-1h /C0 00 00 00 00 30 46 4f 4f 45 52 20 20
0000: Dist-1h /C0 00 00 00 00 30 46 4f 4f 45 52 20 20
0000: 20 30 34 20 42 30 31 33 54 42 20 20 20 20 20
0000: Status /O0
0005: Message-in /C0
0005: Message-in /C0
0005: Message-in /C0
0004: Select w.1Ah /C0
0044: Message-out/CO(Identify)
0045: Command /C06 Read) 00 00 10 01 00
0046: Select w.1Ah /C0
0046: Command /C06 Read) 00 00 10 01 00
0046: Select w.1Ah /C0

Custom Routines Programmable In C
Easily Readable "SCSI English" Display



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1755 E. Bayshore Road, 18A Redwood City, CA 94063

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

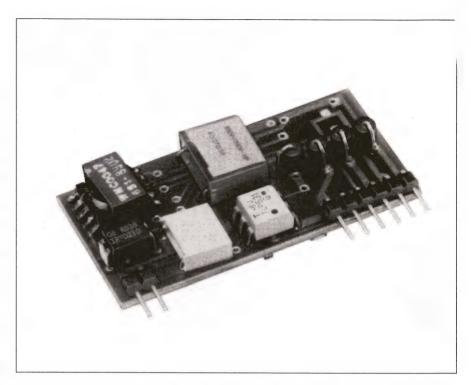
POWER MODULE

- Works directly from a telephone line
- Offers four outputs

The LPM 1000 power-supply module is designed to interface ISDN microelectronics with standard phone power sources. Working directly from a high-impedance telephone line, the module accepts inputs of -28 to -78V dc and outputs $\pm 5V$ at 150 mA and $\pm 11.5V$ at 65 mA. The isolated outputs are fully protected against load failure. Efficiency equals 75% and rated life measures 10 years. The module measures $2 \times 1 \times 0.425$ in. \$31.80 (1000).

Lambda Semiconductors, 121 International Blvd, Corpus Christi, TX 78406. Phone (512) 289-0403.

Circle No 396





Make your big ideas smaller, lighter and brighter.

DURACELL® XL™ DL123A Lithium Batteries give you the power to think small, improve performance and portability.

Today's emphasis on smaller, lighter, more powerful portable devices requires a bright idea in battery technology. It's here.

Size for size, the DL123A delivers more combined power and energy than other consumer replaceable batteries. In fact, for high current applications, this compact 3-volt lithium battery delivers up to four times more energy than a 1.5-volt AA size battery — even more at low temperatures.

COMPONENTS & POWER SUPPLIES



DRIVER KIT

- Evaluates power drivers
- Comes with a fully assembled evaluation board

The TSC442X EV kit allows you to evaluate MOSFET, CCD, and power drivers. It includes a test board, data sheets, a number of the manufacturer's power drivers complete with data sheets, a range of capacitors for load simulation, and an instruction manual. The power drivers include dual-, single-, and

complementary-output devices. The board is fully assembled and tested and includes sockets for the driver and load connections as well as a low-noise connector to interface with a scope. You can evaluate driver devices from any number of vendors so the board can serve as an incoming QC fixture. \$39.

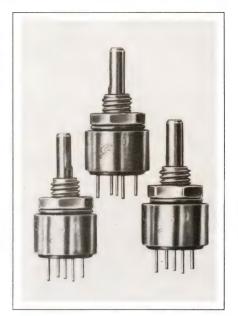
Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94039. Phone (415) 968-9241. FAX 415-967-1590. TWX 910-379-6494.

Circle No 397

ROTARY SWITCH

- Has a binary-coded output
- Features a 25,000-cycle life

Measuring 0.5 in. in diameter, Series 26 binary-coded-output rotary switches are rated for 25,000 cycles of operation when switching logic-level loads. The switches have a 16-



position output, but an adjustable stop feature allows users to create a 10-position BCD output or an 8position octal-code output. Any portion of the standard binary code can be isolated and used as the output



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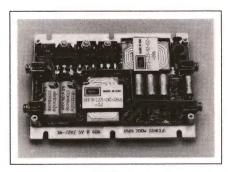
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by adjusting the location of the stops. As a standard feature, all switches come with front-panel seals. \$6.52 (100). Delivery, four to six weeks ARO.

Grayhill Inc, Box 10373, La Grange, IL 60525. Phone (312) 354-1040. FAX (312) 354-2820. TLX 6871375.

Circle No 398



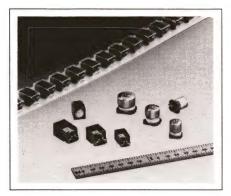
DC/DC CONVERTER

- Available in kit form
- Features 27W/in³ density

Housed in a package measuring $3\times5\times0.5$ in., this dc/dc converter accepts 36 to 72V inputs and delivers a 5V, 40A output-a power density of 27W/in3. Available in assembled or kit versions, the unit owes its small size to the use of planar magnetics. The converter switches at 300 kHz, has an 80% efficiency at full load, and features a total regulation of 1%. The converter features short-circuit protection, current-mode PWM control, 50-mV output ripple, soft start, no minimum load requirement, and 500V input-to-output isolation. All power components are thermally referenced to one base plate/heat sink. This aluminum base plate can be conduction or forced-air cooled. Converter kits include instructions, parts list. schematic. troubleshooting manual. Kit, \$250; assembled version, \$500. Delivery, four to six weeks ARO.

Multisource Technology Corp, 393 Totten Pond Rd, Waltham, MA 02154. Phone (617) 890-1787. FAX 617-890-8011.

Circle No 399



CHIP CAPACITORS

- Designed for solder reflow applications
- Capacitance values range to 100 µF

The units in the MF, MFK, and MVK Series of aluminum electrolytic chip capacitors are designed for solder reflow surface-mount applications. MF and MFK models operate to 85 and 105°C, respectively, and are available with case heights of 3, 4.1, and 4.6 mm. The tubular units in the MVK line are rated for 105°C operation and have a maximum case height of 6 mm. MF and MFK devices have a 4 to 50V dc voltage rating and capacitance values of 0.1 to 68 μF and 0.1 to 47 μF, respectively. MVK modules have capacitance values of 0.1 to 100 µF and voltage ratings of 6.3 to 50V dc. The chips withstand vapor phase and infrared soldering operations. The chips are available on tape-and-reel packaging in 12- and 16-mm widths. \$0.08 to \$0.12. Delivery, stock to 12 weeks ARO.

United Chemi-Con Inc, 9801 W Higgins Rd, Rosemont, IL 60018. Phone (312) 696-2000.

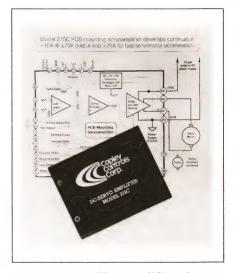
Circle No 400

SERVO AMPLIFIER

- Delivers 25A pk at 75V
- Dissipates only 14W

The Model 215C servoamplifier develops a ± 75 V at ± 10 A continuous 4-quadrant output to provide 1 hp of motion control. The unit also develops ± 75 V at ± 25 A pk to accommodate fast stopping, starting, and

reversing requirements. The amplifier dissipates only 14W at full load, equating to an efficiency of 98%. The unit uses a MOSFET power bridge to develop its 4-quadrant output from a single supply of 25 to 80V dc. An internal dc/dc converter provides all the necessary amplifier operating voltages. Protection circuits provide automatic shutdown in response to overcurrent, overvoltage, and excessive



temperature. The amplifier also responds to logic inputs that control end of travel, beginning of travel, and emergency stop. \$459. Delivery, stock to six weeks ARO.

Copley Controls Corp, 375 Elliot St, Newton, MA 02164. Phone (617) 965-2410. TLX 285975. FAX 617-965-7315.

Circle No 401

DC/DC CONVERTER

- Offers a programmable output voltage
- Efficiency ranges to 90%

In addition to soft start and crowbar load protection, the GS-R400VB dc/dc converter offers a programmable output voltage and selectable current limit. With a suitable variable resistor, you can vary the output voltage between 5.1 and 40V for inputs of 9 to 46V, respectively. Efficiency varies from 75 to 90% within the same output voltage



HEADQUARTERS: Phone. (803) 963-6300, FAX: (803) 963-6521; U.S.A., Newport Beach, CA, Phone: (714) 640-9320. FAX: (714) 720-9807; Santa Clare, CA, Phone: (408) 986-0424, FAX: (408) 986-1442. Irving, TX, Phone: (214) 556-0009. FAX: (214) 401-0254; Schaumburg, IL, Phone: (812) 517-1030, FAX: (312) 517-1037; Stoacham, MA, Phone: (617) 279-0400. Greenville, SC, Phone: (803) 242-5795, EUROPE, Switzerland, Phone: 41-22-39-65-00, FAX: 41-22-33-40-10, Germany, Phone: 49-89-46-30-01; FAX: 49-89-46-04-117. France, Phone: 31-46-377-05-563, FAX: 33-1-49-76-06-63; United Kingdom, Phone: 44-279-757-343, FAX: 44-279-757-186; ASIA, Hong Kong, Phone: 652-3770-5633, FAX: 852-3-770-5635, Singapore, Phone: 653-67-767; FAX: 65-567-1585; Talwan ROC, Phone: 886-2-72-8885, FAX: 886-2-721-3125; Karea, Phone: 62-2-59-8131, FAX: 82-2-2-3-3-806

range. You can also program the output overcurrent limit by using an external resistor whose value is determined by the current limit selected. Minimum output current must equal 100 mA for proper converter operation. Oscillator and synchronization pins allow you to operate the modules in tandem without generating beat frequencies. \$25 (100).

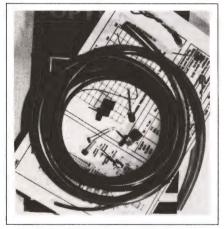
SGS Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX 602-867-6290.

Circle No 402

EXPERIMENTER KITS

- Cover a variety of subjects
- Include all hardware

These kits are designed to provide hands-on experience and the latest theory on fiber-optic communications links. Topics covered include light pipes; multitone modulation of digital transmission; AM fiber-optic



receivers; fiber-optic light-opencable, single, or bidirectional communications; and digital data links. The kits include all necessary hardware such as emitters, detectors, and electronics; and simplex and duplex cables and connectors. All kits contain easy-to-follow instructions and illustrated manuals. \$19.95 to \$54.95.

Sintec Co, Box 410, Frenchtown, NJ 08825. Phone (201) 996-4093.

Circle No 403



LED LAMPS

- Designed for outdoor applications
- Feature a 410-mcd luminous intensity

Suitable for use in outdoor applications, the AND180PGP high-intensity lamp features a T1-3/4 green LED in a water-clear plastic package. A drive current of 20 mA produces a typical luminous intensity of 410 mcd. Peak wavelength equals 567 nm, and maximum power dissipation is 120 mW. Although the lamp is primarily aimed at outdoor applications involving message indicators, you can also use the 180PGP to backlight display panels and panel-mounted switches. \$0.85 (1000).

AND, Box 4188, Burlingame, CA 94011. Phone (415) 347-9916. FAX 415-340-1670. TLX 6771439.

Circle No 404

DIP SOCKETS

- Available with self-retaining solder tails
- Offer from 8 to 48 contact positions

SDL Series DIP sockets feature dual-leaf side-wiping contacts to minimize contact resistance, and overstress protection to prevent contact damage. Offering a choice of standard or self-retaining solder tails, the sockets are available in sizes ranging from 8 to 48 contact positions. Rated for 1A and 250V ac, the sockets feature black polvester insulators that have a 94V-0 UL rating; the phosphor bronze contacts are plated with 150 min. of tin over 75 min. of nickel. The sockets meet the material requirements of Table 23.1 of the UL 1410 standard for TV receivers and video equipment. \$0.006/contact position (1000).

Circuit Assembly Corp, 18 Thomas St, Irvine, CA 92718. Phone (714) 855-7887. FAX 714-855-4298.

Circle No 405



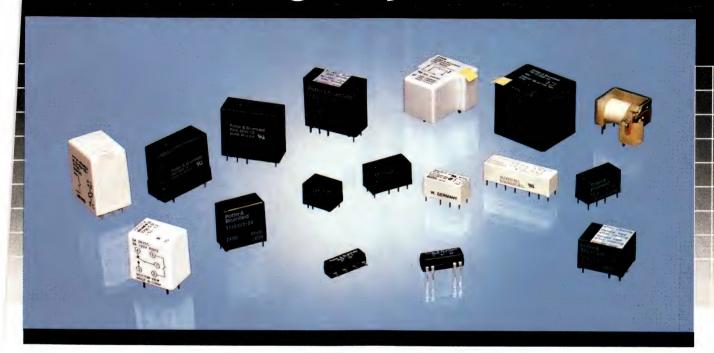
TEST FIXTURE

- Eases chip-capacitor measurements
- Designed to ease chip placement The CCT-100 test fixture is a bench tool that's designed to measure rectangular chip capacitors. The design features a spring-loaded mechanism that holds the chips and ensures a positive contact. An enclosed phenolic cavity eases chip placement. The fixture features nickel-plated contacts and holds capacitors with widths ranging from 0.01 to 0.375 in. A battery nut allows you to make the required width adjustments. The CCT-100 plugs into the standard 0.075-in. banana jack of a handheld capacitance meter; you can zero out fixture capacitance using the meter. \$79.95.

Lark Engineering Co, 27151 Calle Delgardo, San Juan Capistrano, CA 92675. Phone (714) 240-1233. FAX 714-240-7910.

Circle No 406

Specify P&B for dry circuit to 30A load switching on your P.C. board.



New Models Expand Offering

Potter & Brumfield's expanded line of printed circuit board relays provides the features you need — whether you're switching dry circuits or 30A loads. New products, traditional P&B quality and unbeatable service combine to help solve your toughest relay design-in problems in telecommunications, appliance, industrial control and other applications.

Miniature Relays Switch 1mA to 10A

New T73 and T74 series miniature P.C. board relays join the T70 series as Potter & Brumfield's low-cost SPDT units for general purpose applications. Various contact materials permit these immersion cleanable relays to switch from 1 mA through 10A. Sensitive coil models are available.

Expanded Line of 4,000V Isolation Relays

Extensions to the line of RK series relays feature 8mm coil-to-contact spacing for 4,000V isolation. SPDT models switch loads to 20A, while DPDT models switch up to 5A. Both sealed and unsealed types are now offered with either AC or DC coils.

T90 & T91 - 30A Workhorses

T90/T91 series relays have SPDT contacts for loads to 30A. The DC coil T90 is offered as an open-style

or sealed relay. The T91 is available with a DC coil, and it's offered with quick connect terminals for load connections. An AC coil T91 will be available soon.

More Models for Low Signal Switching

The growing line of P&B low-signal relays features units with single or multiple contacts to provide dependable switching of 2A and under loads. Both polarized and non-polarized units are offered in various coil sensitivities. Included are immersion cleanable DIP and SIP types.

Stock Availability

Many models are available off-the-shelf from your authorized P&B distributor. Of course, distributor stock is backed by Potter & Brumfield's extensive factory inventory.

Find Out More

Contact us today for information on our complete line of P.C. board relays. Potter & Brumfield, A Siemens Company, 200 S. Richland Creek Drive, Princeton, Indiana 47671-0001.

Call toll-free 1-800-255-2550 for the P&B authorized distributor, sales representative or regional sales office serving your area.

Potter & Brumfield A Siemens Company

8905

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and have rotational lives in the millions.

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CIRCLE NO 22

DID YOU KNOW?

EDN is distributed at every major electronics/computer show in the U.S., France, and Germany.

COMPONENTS & POWER SUPPLIES

MODULATORS

- Have a 5:1 frequency range
- Operate over a 55 to +100°C range

The design of these quadrature PSK modulators combines ferrites with coupled-line techniques to achieve multi-octave performance. The PMQPW-150 covers a range of 30 to 150 MHz, and the PMQPW-250 operates over a 50- to 250-MHz range. Each has an amplitude imbalance of <0.4 dB and a phase imbalance of <3°. Over an operating range of -55 to +100°C, changes in insertion loss, phase imbalance, and amplitude imbalance equal ±1 dB, $\pm 1^{\circ}$, and 0.3 dB, respectively. Both models meet MIL-M-28837 requirements and are hermetically sealed. \$172.95.

Mini Circuits Laboratory, 2625 E 14th St, Brooklyn, NY 11235. Phone (718) 934-4500.

Circle No 407

PHOTOSENSOR

- Features electronically isolated output
- Sensing capability ranges to 17 ft The Decout (decoupled output) photoelectric sensor features an output that is electronically isolated from both the supply and the detector circuits. The unit is available in reflective, direct reflective, throughbeam, and fiber-optic models with sensing ranges from 5 mm to 17 ft. The optical lenses are molded as a single piece that accommodates an infrared filter. The output is a solidstate switch that can supply a load of 100 mA. By inverting the supply voltage connections. vou achieve four output configurations—npn NO or NC, and pnp NO or NC. The unit is hermetically sealed to withstand harsh environments. From \$43.50.

FSI International Inc, 666 Western Ave, Lombard, IL 60148. Phone (312) 932-8866.

Circle No 408

New VR rechargeables improve performance and lower your costs.



Varta's new VR rechargeables permit improved charging rates: both trickle and overcharge. This provides new benefits: the opportunity to reduce costs by simplifying circuitry, and enhanced overcharge protection.

EDN September 28, 1989

Cost reduction of circuitry: Until now, typical NiCd button-cell charging circuits have had two steps...charge at 0.1 CA (14-16 hours) and trickle charge at 0.01 CA (100 hours) while delivering a 5-to-6 year life. The new VR's can be used in this two-step circuitry. However, you can simplify your charging circuitry to one step, and reduce costs accordingly, by designing to both charge and trickle charge at .05 CA (only 25 hours from full discharge to full charge). The VR's will still provide 5-to-6 year life.

Improved overcharge protection.

To handle user abuse or unusual conditions, the new VR's can be charged periodically at up to 0.2 CA (7-hour rate), while providing a useful life of up to six years. They can even be overcharged at 0.2 CA (room temp.) for one whole year. VR cells are dimensionally the same size as the DK cells they replace. Initial capacities (mAh) being

phased in are 60, 100, 170 and 280 (replacing the 250). Available in a wide variety of Varta battery packs and connections. For this literature on the VR series or for information on all Varta batteries, please call 1-800-431-2504, Ext. 260. Or write to Varta below.



205



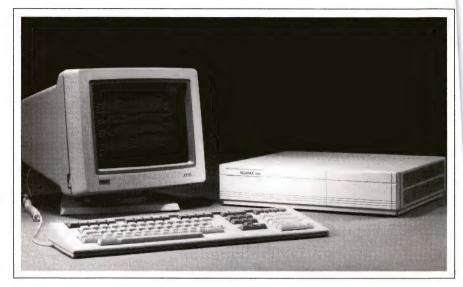
NEW PRODUCTS

COMPUTERS & PERIPHERALS

VAX COMPUTER

- Features the CVAX μP and as much as 16M bytes of RAM
- Has built-in standard and ThinWire Ethernet interfaces

A member of the VAX computer family, the MicroVAX 3100 replaces the MicroVAX 2000 by providing more performance features at a lower price. It features the CVAX µP, which is used in the MicroVAX 3300 and 3400 systems; as much as 16M bytes of memory; and a built-in standard and ThinWire Ethernet interface. The computer comes in two models that run either the VMS or Ultrix operating systems. The minimum configuration for the Model 10 is 4M bytes of memory, a 104M-byte hard-disk drive, a 1.4M-byte, 3½-in. floppydisk drive, four asynchronous serial ports, and a 5-user VMS operating system with a DECnet end-node



software license. The minimum configuration for the Model 20 contains 8M bytes of memory, two 104M-byte, hard-disk drives, eight asynchronous and one synchronous serial ports, a 95M-byte streaming-cartridge tape drive, and a 10-user

VMS operating system with a DECnet end-node software license. Model 10, \$8480; Model 20, \$22,965.

Digital Equipment Corp, Maynard, MA 01754. Phone (508) 493-6915.

Circle No 386

ETHERNET INTERFACE

- Uses a Macintosh computer's built-in SCSI port
- Compatible with EtherTalk network software

The Ether+ is a stand-alone Ethernet interface for Macintosh computers and connects to any MAC with a built-in SCSI port. The unit is fully compatible with Apple's EtherTalk network software-driver specification so it operates with popular network packages such as TOPS, AppleShare, Novell Macintosh, and Telnet. Because AppleTalk communicates approximately 40 times slower than the 10M-bps rate of Ethernet, the network protocol does not achieve the full Ethernet data rate. The unit provides both thin Ethernet and thick Ethernet connections by adhering to IEEE-802.3 10Base2 and 10Base5 standards, respectively. A back-panel switch selects a SCSI address number. The enclosure measures $5.5 \times 1.5 \times 7.5$ in. and uses a 20W wall-mount power supply. \$495.

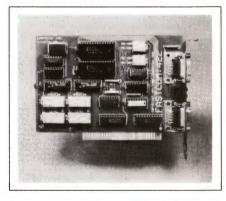
Compatible Systems Corp, Drawer 17220, Boulder, CO 80308. Phone (800) 356-0283; in CO, (303) 444-9532. TLX 249643.

Circle No 387

RS-422/485 BOARD

- Uses Intel's 82050 UART
- Operates with MS-DOS, Microsoft Xenix, and SCO Xenix

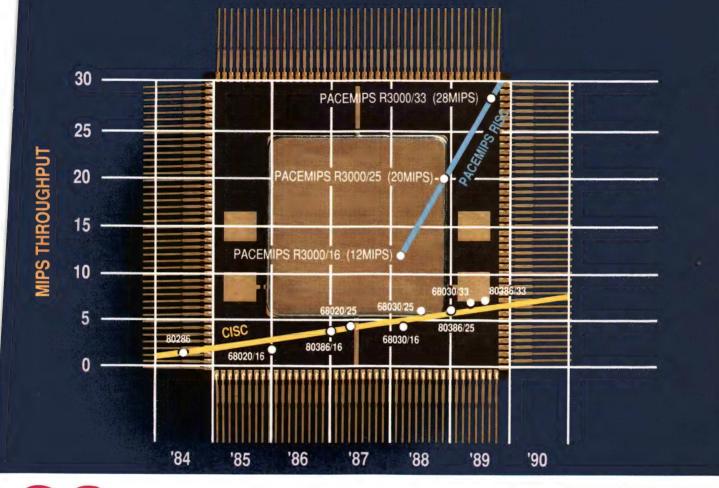
The Fastcom:422 is a single- or dual-channel RS-422/485 interface board for IBM PC, PC/XT, PC/AT, and compatible computers. Operating with MS-DOS, Microsoft Xenix, SCO Xenix, and most programs, the board uses the COM1 or COM2 port. Other features include dual DB-9 connectors, RFI shielding, and RTS/CTS control signals. The standard version contains an Intel 82050 UART, which is a low-power



equivalent of the 16450 UART. The unit also comes with an option for an Intel 82510 UART, which features two software selectable modes: an 82050-compatible mode and a high-performance mode. The high-performance mode offers baud rates as high as 288k baud, a 4-byte receive-and-transmit buffer, two separate baud-rate generators that permit transmission and reception at different baud rates, and control character recognition. A Commbios/ Commbuff communications-soft-

Performance's 33/25 MHz PACEMIPS RISC Smashes CISC Price/mip

CMOS PACEMIPS RISC components sell for approximately the same price as CISC. PACEMIPS price/mip is 1/4 that of CISC.



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A new single chip component to perform the main memory read and write buffer functions will be available in early 1990. Increased integration and lower power lead to effective system design and board density.

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CIRCLE NO 112

ware development tool comes with the board. Fastcomm:422, \$375; optional 82510, \$25; second channel option, \$49.

Commtech Inc, 8622 Mt Vernon Ct, Wichita, KS 67207. Phone (316) 651-0077.

Circle No 388



ARCNET BOARD

- Uses the SMC9026 VLSI controller
- Selectable base address on 4kbyte boundaries

The S-ARC-01 Arcnet interface board for the STE Bus uses Standard Microsystem's SMC9026 VLSI controller and acts as an intelligent slave. The base address is selectable for any 4k-byte boundary within the short I/O base. The controller's firmware provides tokenpassing, media-access control, as well as data-link features. Besides communicating at the standard 2.5M-bps Arcnet rate, the board operates with the 20M-bps Arcnet rate announced by the Arcnet Trade Association. The board has 2k bytes of dual-ported RAM, provides four which 512-byte packet buffers. The card uses Arcnet cable transceivers that link to a network cable via a BNC connector on the front panel. The board comes with network drivers running under MS-DOS and has an option for NetBIOS. \$858.

C&C Technology Inc, Bldg 9, Unit 60, 245 W Roosevelt Rd, West Chicago, IL 60185. Phone (312) 231-0015. TLX 4974811. FAX 312-231-0345.

Circle No 389



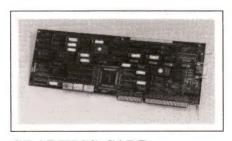
NETWORK SERIES

- Consists of 1-board hardware for data communications
- Operates as gateways, FEPs, bridges, or hub switches

The CPS1000 series of single-board hardware systems for data communications lets you customize LAN gateways, front-end processors, bridges, packet assemblers/disassemblers, or hub switches for networking applications. The systems can simultaneously operate with multiple protocols including X.25, TCP/IP, Ethernet, and token ring. You can independently configure its serial ports as RS-232C, RS-449, RS-530, or V.35 interfaces. The systems incorporate custom VLSI circuitry for tailoring to a specific application. \$1500 to \$9300. Delivery of initial product, 120 days ARO.

SBE Inc, 2400 Bisso Ln, Concord, CA 94520. Phone (800) 221-6458; in CA (800) 328-9900. FAX 415-680-1427.

Circle No 390



GRAPHICS CARD

- Allows windowing on a 1280×1024 monitor
- Runs EGA, MDA, CGA, and Hercules software

When used in conjunction with the company's UDC-2600 graphics controller board, the MegaVu IBM VGA graphics card for the IBM PC/AT and compatible computers lets you display a VGA window on a

 1280×1024 monitor. The board VGA application runs a 640 × 480-pixel resolution and transfers the data via a 10-MHz external bus to the controller board for display on the monitor. The user can simultaneously display 1280×1024 images and VGA windows. You can view a VGA application in two modes: either a 640×480-pixel quadrant of the 1280×1024 display or the entire screen area. In addition, the board runs MDA-, CGA-, and Hercules-compatible software. A DMA controller transfers data over the 10-MHz bus into the display memory on the controller card. \$1195; 2-board set, \$4470.

Univision Technologies Inc, 12 Cambridge St, Burlington, MA 01803. Phone (617) 273-5388. TLX 988755.

Circle No 391

VOICE RECORDER

- Digitally stores audio messages as long as 128 sec
- Samples audio signals from 16 selectable channels

The DVR digital voice recorder samples and digitally stores data from 16 selectable channels. The $2\times2\times1$ -in, stand-alone board contains 1M byte of dynamic RAM, which provides the following recording times at the specified sampling rates: 128 sec at 8k bps, 98 sec at 11k bps, 65 sec at 16k bps, and 35 sec at 32k bps. The board weighs 1 oz and has four corner holes for mounting. It requires an unregulated 8 to 12V dc supply and draws <4 mA in a standby mode. The unit also contains a 600Ω to 10 $k\Omega$ microphone, a 1W audio-output amplifier, and a green LED status indicator. All input and output lines connect to solder pads for interfacing with a remote controller. DVR-4, \$59.50; DVR-16, \$97.50.

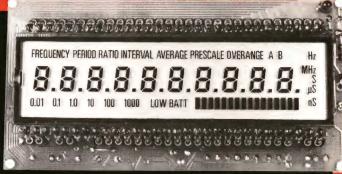
Electronic Devices & Engineering Co, Box 1872, Palm Springs, CA 92262. Phone (619) 320-8880.

Circle No 392

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WORLD'S FIRST

High Performance Universal Counter Timer Module/Panel Meter



ACTUAL SIZE

- 10 Digit (120 Segment) LCD Display with Gate, Function, and Input Annunciators.
- .1 Hz to Over 150 MHz Direct Count (1 Hz resolution in 1 Sec).
- Single Shot Time Interval 100 ns, .1 ns averaged.
- Functions Include: Frequency, Period, Ratio, and Time Interval and Average.
- 16 Segment Analog Input Bargraph is driven by an 8 Bit A to D and Can Be Used for Signal Level Display.
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CIRCLE NO 23

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Universal MultiProgrammer™

DATA I/O 288* Performance PLUS PLD Support !!



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135H-U with optional LOGICel.

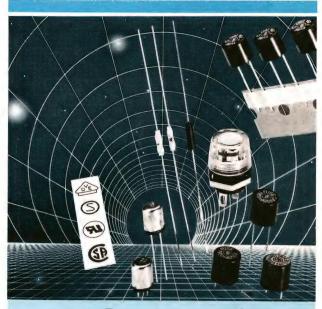
- ★ Model 135H is a GANG & SET (E) EPROMProgrammer.
- ★ Programs virtually all EPROMs & EEPROMs up to 2048K.
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INTERNAL MODEMS

- Have MNP class 1 to 5 ECC
- Fit a full-sized expansion slot and operate with MS-DOS

Three internal modem cards for IBM PC, PC/XT, PC/AT, and compatible computers have MNP class 1 through 5 error-correction code and data compression. The Courier HST/PC modem features the company's proprietary asymmetrical modulation technique operating at speeds as high as 14,400 bps. Using MNP class 5 data compression, the unit achieves an effective throughput of 26,000 bps. In its high-speed mode, this model features a 450-bps reverse channel for full-duplex communications. The Courier VC.32/ PC is compatible with the CCITT V.32 standard for 9600- and 4000bps communications. The modem achieves an effective throughput of 17,400 bps with MNP class 5 data compression. The Courier HST dual

standard/PC modem combines all the features of the other two modems into one. The modems fit any full-sized expansion slot and operate with MS-DOS. All three units conform to the CCITT V.22 bis, V.22, and V.21 specifications as well as the Bell 212A and 103 standards. Courier HST/PC, \$895; Courier V.32/PC, \$1349; Courier HST dual standard/PC, \$1395.

USRobotics Inc, 8100 N McCormick Blvd, Skokie, IL 60076. Phone (800) 342-5877; in IL (312) 982-5001; in Canada (800) 553-3560.

Circle No 393

IPI CONTROLLER

- Manages the operation of 32 disk drives
- Uses from two to four IPI-3 host channels

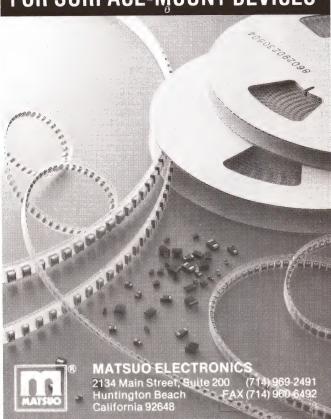
The ArrayMaster 9058 intelligent peripheral-interface (IPI) controller

manages as many as 32 disk drives using two to four IPI-3 host channels and four IPI-2 drive ports. The controller can handle a 25M-byte/ sec burst-transfer rate from the host and transfer data at 10M bytes/ sec to the disk drive. The controller has four 128k-byte data buffers, 1 per drive port. The unit comes mounted in the company's Sabre 8in. enclosure that includes a power supply and a cooling fan, and it meets UL, CSA, VDE, and FCC class B requirements. In addition, the controller uses a modified 96-bit Reed-Solomon error-correction code. Controller with two IPI-3 channels and four IPI-2 ports, \$10,250 (OEM qty). Evaluation units available in October.

Imprimis Technology Inc, 12501 Whitewater Dr, Minnetonka, MN 55343. Phone (612) 936-6267.

Circle No 394

TANTALUM CHIP CAPACITORS FOR SURFACE-MOUNT DEVICES



CIRCLE NO 26

COPROCESSOR BOARD

- Uses a 32-bit Am29000 RISC CPU
- Has 6M bytes of cache memory The enhanced Nusuper coprocessor board for the Macintosh computer uses a 32-bit RISC CPU and a 50-MHz system clock to deliver 25 MIPS peak and 17 MIPS sustained. The board features as much as 6M bytes of cache memory, and it can access 32M bytes of dynamic RAM on the Nubus. When operating in a bus-master mode, it has direct access to graphics and other I/O cards on the bus. The company supplies the Metaware compiler and other development tools including an assembler, a linker, and a debugger. In the Multifinder mode, you can install as many as four boards in a single host. An Am29027 floatingpoint unit is available as an option. 3M-byte version, \$2800 (OEM qty).

Yarc Systems Corp, 5655 Lindero Canyon, Suite 721, Westlake Village, CA 91362. Phone (818) 889-4388.

Circle No 395

The Analog ASIC Solution



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Raytheon's RLA Linear Array Family of user-configurable macrocell arrays—and full design support. (RLA 40, 80, 120, and 160)

- ☐ Configurable macrocells: 4, 8, 12 or 15 gain blocks that can be configured into a variety of analog functions to achieve your system's needs.
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□ And more: Choose from a wide variety of packages including plastic and ceramic DIPs, SOICs, PLCCs, and LCCs in commercial, industrial and military temperature ranges.

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Ventana Press, Box 2468, Chapel Hill, NC 27515.

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Superconductor Applications Association, 24781 Camino Villa Ave. El Toro, CA 92630.

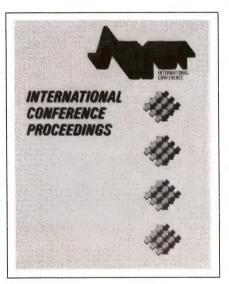
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Books deal with VHDL and its applications

The VHDL Handbook is a 416-pg working reference for hardware designers. Its "cookbook" approach provides examples that illustrate features of the VHDL language and show how you can model particular classes of hardware devices in VHDL. \$65. The 317-pg VHDL: Hardware Description and Design is an introduction to VHDL, investigating specific language constructs. It provides a full explanation of the IEEE 1076 standard for VHDL. \$55. Finally, the 224-pg ASIC System Design with VHDL: A Paradiam deals with the challenge of designing single-chip processors to execute specific application algorithms. To this end, the book attempts to provide a better understanding of interactions among robotic algorithms, computational architectures, and the implementing technology. \$52.50.

Kluwer Academic Publishers, 101 Philip Dr, Assinippi Park, Norwell, MA 02061.

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Conference proceedings span wide range of industries

The Asyst '88 International Conference Proceedings present 48 application articles on PC-based scientific and engineering applications. It covers such topics as data analysis, biomedics, chemistry, instrumentation control, materials research, physics, and testing. Each article describes a particular project, reports on the hardware and software used, and provides the conclusions of the researcher. The applications range from theoretical modeling to automated testing to computer-aided instruction. \$25.

Asyst Software Technologies Inc, 100 Corporate Woods, Rochester, NY 14623.

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Note describes custom switch matrixes

A product note, entitled HP 8760 Custom Switch Matrixes for Microwave ATE, discusses the manufacturer's capabilities for producing and testing complex switching assemblies. The publication details matrix theory and practice, from 1-channel matrixes to more complex full-access models with numerous inputs and outputs. Other details include performance specifications and how to document test procedures and construction. The note also provides further suggestions for internal self-test procedures.

Hewlett-Packard, 19310 Pruneridge Ave, Cupertino, CA 95014.

Circle No 367

How to hasten IEEE-488 application programs

This 8-pg application note, *Programming with NI-488 Software*, explains how to increase throughput and reduce development time for IEEE-488 application programs. The note also contains examples that highlight some of the software features.

National Instruments, 12109 Technology Blvd, Austin, TX 78727.

Circle No 368

Study surveys overseas CASE markets

This major multiclient study on the budding market for computer-aided software engineering (CASE) products in Europe and Japan comprises three volumes. Volume 1 focuses on the European market, where two companies—CGI Informatique of France and Softlab of Germany—are the two leading manufacturers of CASE tools for management-information-system/data-processing applications. Volume 2 concentrates



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Strategic Focus, 500 E Calaveras Blvd, Suite 321, Milpitas, CA 95035.

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Listing of PowerMOS transistors on disk

The vendor's comprehensive list of PowerMOS transistors is available on floppy disk, allowing you to search quickly for a specific type number, as well as for comparative data of competitors. You can use the disk on IBM PCs and most compatible computers. A set of instruc-



tions guides you in the use of the disk.

Philips Components, Box 218, 5600 MD Eindhoven, The Netherlands.

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Amperex Electronic Corp, Providence Pike, Slatersville, RI 02876.

Circle No 370

Catalog covers electronic materials

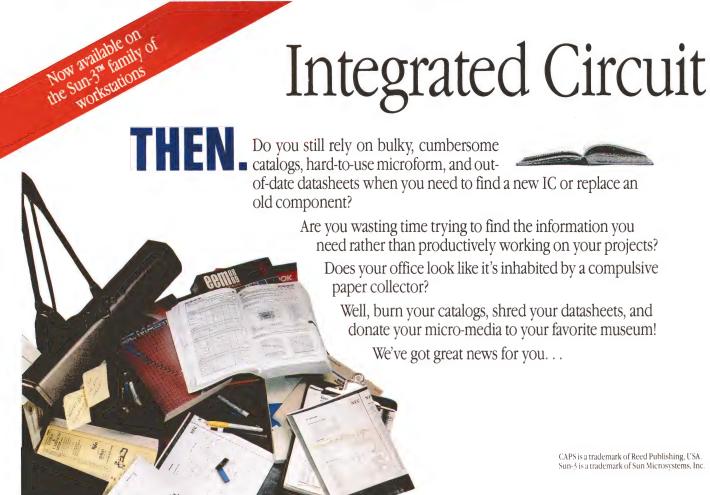
This 120-pg premiere issue describes products for static control; EMI/RFI shielding; wire and harnessing products; identification systems; thermal interface materials; adhesives, coatings, and encapsulations; solder products and pc-board chemicals; pressure-sensitive tapes; film insulating products; and fabricated parts.

Electrical Insulation Suppliers Inc, 300 N Mannheim Rd, Hillside, IL 60162.

Circle No 371

Electronic cataloging of trimmers

The SpecTrim electronic catalog is on an IBM PC-compatible 5½-in. floppy disk and comes with a 22-pg user's guide. You can pinpoint the optimal trimmer for your applica-



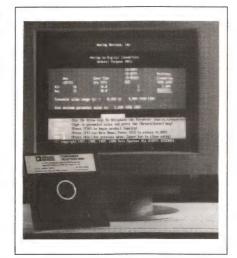
tion and select from a base of 8600 standard part numbers or from performance parameters. Another feature allows you to cross-reference trimmers of the company's model with those of other manufacturers. The disk also features helpful terms and definitions.

Bourns Inc, 100 Columbia Ave, Riverside, CA 92507.

Circle No 372

Disk guides you to optimal components

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this listing you can look up the data sheet of each component for further details. This database search lets you see the potential cost vs performance tradeoffs.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton MA 02021.

Circle No 373

Spice macromodels noted

Three application notes explain the company's OP-64, OP-42, and OP-400 Spice macromodels. The publications point out several improvements: The models concentrate on frequency poles and zeros that determine the frequency of op amps; the macromodels do not require internal grounds; and in the new models, all currents are accounted for in the output stage. AN-110 describes the Spice macromodel for the OP-64 high-speed, wideband op amp; AN-117 explains the Spice macromodel for the OP-42 highspeed, fast-settling precision op amp; and AN-120 discusses the Spice macromodel for the OP-400 quad low-offset, low-power op amp. The notes all provide schematics, graphs, and listings.

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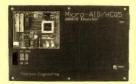
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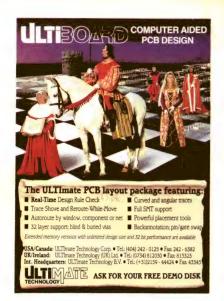


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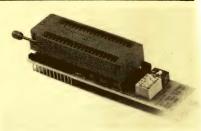
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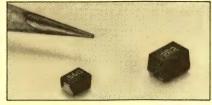
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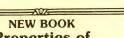
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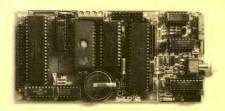


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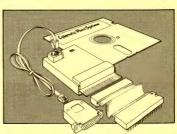
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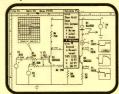
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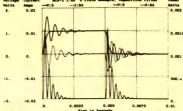
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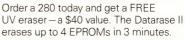
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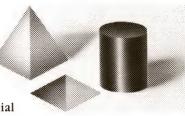




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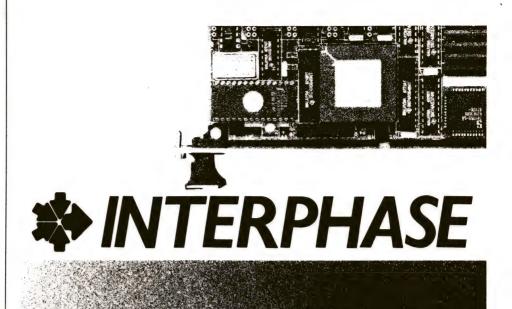
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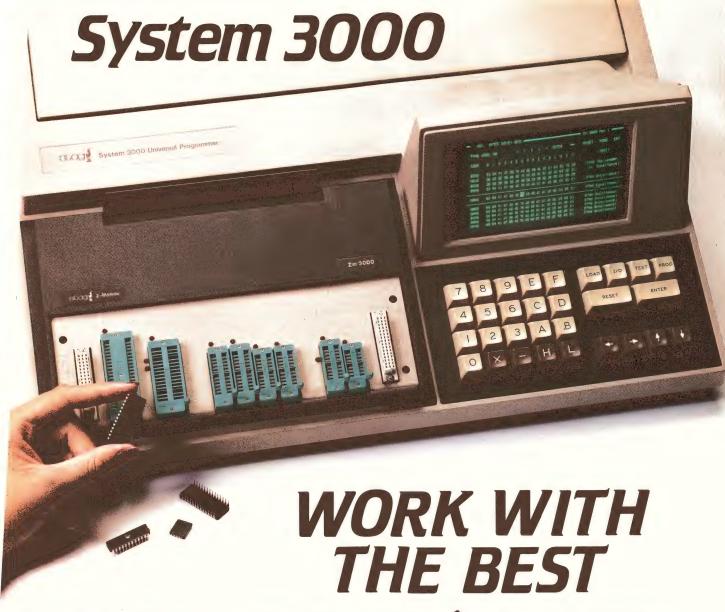
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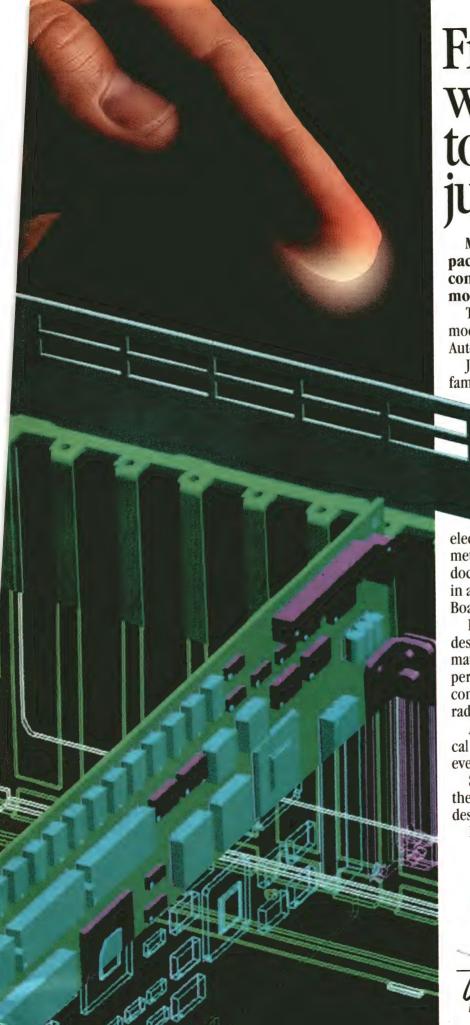
FBR46	Relay Specifications				
Contact Arrangement	DPDT (2FORMC) bifurcated contact				
Maximum Switching Power	30W, 60VA				
Contact Resistance	100mΩ max. (initial value at 6VDC, 0.1A)				
Coil Power Consumption 150mW					
Insulation Resistance	100MΩ min. (at 500VDC)				
Dielectric Withstand Voltage	1000 VAC (for 1 min.)				
Surge Voltage	1500V (between open terminals)				
Electrical Life	DC: 200×10 ³ ops. min. (at rated coil load) AC: 100×10 ³ ops. min. (at rated coil load)				
Operating Temperature	-30°C to 70°C				
Size	L: 15.8mm (0.620 in.) W: 9.7mm (0.382 in.) H: 7.8mm (0.307 in.)				



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LOOKING AHEAD

EDITED BY JAMES P SCANLAN

US electronic shipments increase 5.3% from mid-1988

Despite predictions of a slightly slowing economy, US factory shipments of electronic equipment, components, and related products totaled \$127.7 billion for the first half of 1989, excluding imports, according to the Electronic Industries Association (EIA) (Washington, DC). Last year's first-half figure was \$121.2 billion.

The largest percentage increase was realized in the sale of electronic components, which totaled \$25.9 billion, more than 8% higher than last year's \$24 billion. Next came consumer electronics, which increased 6.4% to \$15.2 billion. Shipments of communications equipment rose 4.8% to \$33.2 billion from last year's \$31.7 billion, and sales of computers and industrial-sector

MID-1989 US FACTORY SALES OF ELECTRONIC PRODUCTS (BILLIONS OF DOLLARS)

	ELECTRONIC COMPONENTS	CONSUMER* ELECTRONICS	COMMUNI- CATIONS EQUIPMENT	AND INDUSTRIAL- SECTOR PRODUCTS	OTHER ELECTRONICS- RELATED PRODUCTS/ SERVICES	TOTAL
MID-1989	\$25.9	\$15.2	\$33.2	\$41	\$25.1	\$127.7
MID-1988	\$24	\$14.3	\$31.7	\$39.5	\$23.8	\$121.2
PERCENT CHANGE	8%	6.4%	4.8%	4%	5.4%	5.3%

*INCLUDES IMPORTS AND FACTORY SALES OF PRODUCTS NOT CLASSIFIED AS CONSUMER ELEC-TRONICS BY THE DEPARTMENT OF COMMERCE.

**TOTAL DOES NOT EQUAL THE SUM OF INDIVIDUAL PRODUCT GROUPS DUE TO OVERLAPPING OF PRODUCT GROUPS AND THE EXCLUSION OF CONSUMER-ELECTRONICS IMPORTS.

(SOURCE: ELECTRONIC INDUSTRIES ASSOCIATION)

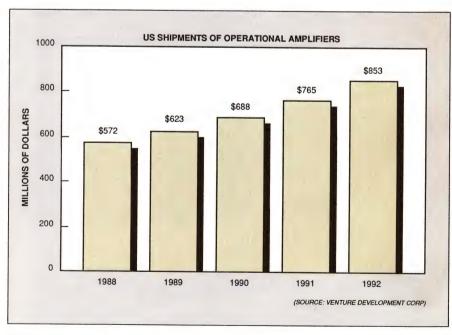
products increased by nearly 4% to \$41 billion.

The sale of other electronic-related products and services totaled \$25.1 billion—a 5.4% jump over last year's figure. According to EIA, approximately 21% of the total US electronic shipments over the first half of this year—approximately \$27 billion—were composed of defense electronics.

High performance boosts demand for op amps

The growing need for higher precision is spurring sales of op amps. Meeting this need are high-performance op amps, which are becoming increasingly popular. In virtually all areas of op-amp performance, demand for high-performance devices will outpace the consumption of their standard counterparts, according to Venture Development Corp, a management consulting company based in Natick, MA. Opamp revenues could reach \$623 million this year, with high-performance types accounting for incrementally larger shares of overall op-amp revenues. These revenues are predicted to reach \$853 million by 1992.

Op amps with offset voltages at or below 1 mV currently account for more than 25% of the generated dollar volume. Applications for these op amps include automatic



test equipment, industrial process controls, industrial data-acquisition systems, and medical instrumentation.

Roughly 17% of op amps shipped

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typ

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10-100MHz

10-100MHz

VSWR(ON)

100-1500MHz

1500-3000MHz

Switching Time (µsec)

(from 50% TTL to 90% RF

Oper. Temp.(°C)

Stor. Temp.(°C)

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1500-3000MHz

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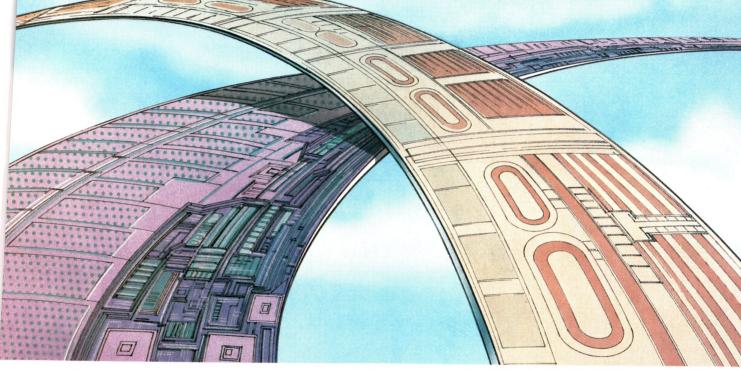
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